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MODEL 851-D
LOGIC ANALYZER

OPERATING AND SERVICE MANUAL

MP MASTER
MA34613

biomation

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OPERATING AND SERVICE MANUAL

MODEL 851-D

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SECTION I

GENERAL INFORMATION

1.1 Certification

Biomation Corporation certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages.

1.3 Instrument Description

The 851-D Logic Analyzer is a new instrumentation tool for the design and repair of digital logic circuits. Complex logic timing relationships can be conveniently recorded, displayed, and analyzed. Eight channels of digital information can be recorded and monitored at rates up to 50 MHz.

The Biomation Model 851-D is designed specifically for analysis of digital logic circuits and signals. The unit can be used on both synchronous and asynchronous signals and can detect random logic pulses as narrow as 5 nsec with the use of the "LATCH" input feature.

The Model 851-D Logic Analyzer provides the ability to measure up to eight digital signals against a preset threshold, update the detectors with an internal or external clock, and store 512 such simultaneous decisions for each input signal. Threshold settings are independently selectable for Channels 1-4 and 5-8. This information is then presented for display

on an oscilloscope in an eight trace timing-diagram presentation. Thus, the user can capture unique combinations of digital events for concise and rapid analysis.

Specifications for the Model 851-D are given in the following paragraphs.

1.4 Specifications

SIGNAL INPUTS

Number. 8.

Impedance. 1 MΩ/10 pF. Inputs greater than ±12 V clamped to ±12 V through 10 kΩ.

Two Threshold Controls. Channels 1-4 independent from Channels 5-8. Selectable TTL, ECL, MST, +0.25, -0.25, and +0.20 V. Continuously variable ±2.4 V. Selectable for X1 or X10 probes.

Max Overload Voltage. ±50 V continuous, ±100 V transient.

Input Modes. Selectable; SAMPLE or LATCH.

Sample Mode. Unit stores the detected logic level present at each positive clock transition simultaneously on all input channels. Maximum channel-to-channel time skew of this clocked data is <1 nsec. Minimum pulse width always detected and recorded is one clock plus 2 nsec with 250 mV or more threshold overdrive.

Latch Mode. Threshold detector latches in state opposite that stored at previous clock transition in the event that multiple transitions of the threshold occur prior to the next clock transition.

Minimum Pulse Width to Latch. 5 nsec with typically 250 mV overdrive beyond actual threshold.

CLOCK

Internal. Selectable 0.02, 0.05, 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, microseconds or milliseconds clock intervals.

External. Via front panel BNC connector, continuous rates from 50 MHz to DC. External clock signal threshold set on threshold selection for Channels 5-8. Positive or Negative edge may be selected. 1 MΩ input. Fixed delay between input data signals and external clock input at the threshold detectors is typically 13 nsec.

TRIGGER

Source. Selectable; internal, external, or manual.

Internal. Combinational triggering; Selectable "1, Don't Care, or 0" for all eight channels. May be triggered when selected combination appears at inputs or triggered when combination disappears from the eight inputs.

External. Via rear panel BNC connector, ECL level or I/O connector, TTL level.

Static Delay. With Delayed Record mode selected and the settable Trigger Delay at zero, the fixed delay between the detected trigger and the first stored data in the memory is 4 sample intervals.

Jitter. Data from repetitive record cycles with respect to the input signals will exhibit 1 clock interval maximum time jitter.

MEMORY

Size. 8 X 512 bits.

Record Mode. Selectable Pretrigger and Delayed record modes.

Pretrigger. Start via front panel momentary ARM switch, auto start selection or via rear panel BNC, ECL level or via TTL level into I/O connector. 0-500 pretrigger samples. Stop via trigger detection and after selectable delay, or via front panel momentary switch.

Delayed. Selectable trigger delay via front panel decade switches to 9999 clock periods, in single clock increments. Record starts after trigger delay has elapsed and stops when 512 bits per channel have been recorded.

DISPLAY OUTPUTS

X Output. Repetitive 1 V p-p ramp waveform 2 msec period.

Y Output. Repetitive 1 msec stair step ramp, each step equally spaced in amplitude. Data for each channel modulates each respective step level.

X1 expansion outputs 500 bits per line. Full range nominally 0 to +1 V.

Z Output. Nominal zero to +5 V pulse. 1 msec wide synchronized with X ramp.

$\overline{Z}$ Output. Nominal +5 V to zero pulse. 1 msec wide synchronized with X ramp.

Cursor. Movable display cursor.

Expansion. X5, X10, X20 full expansion or mixed expansion. Mixed expansion X1 to left of movable cursor and X5, X10, or X20 expand to right of cursor.

DIGITAL INTERFACE

Data. Output, 8 bits parallel, TTL levels positive true, word serial asynchronous data transfer under control of Flag and Command signals. Rates 30 kHz down to DC.

Flag. Output of positive TTL transition indicates data word on output lines can be read. Minimum pulse width 2 μsec.

Command. Input of negative TTL transition requests next data word. Minimum pulse 3 μsec.

Output Request. Input of TTL low or ground stops the display and initiates the digital data output.

Internal Clock Input/Output. Used for connecting several 851-D units together for synchronous recording, ECL level.

Internal Clock Input/Output. Used for connecting several 851-D units together for simultaneous triggering, ECL level.

Internal Arm Input/Output. Used for connecting several 851-D units together for synchronous arming, ECL level. TTL remote ARM also available.

MISCELLANEOUS

Operating Temperature Range: 0-50°C.

Power: 115 V/230 V RMS, 50-60 Hz.

Size: Height: 5.2 in. (13.2 cm). Width: 12.75 in. (32.4 cm). Depth: 19.0 in. (48.3 cm).

Weight: Approximately 25 lbs. (11.3 kg).

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model 851-D.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or Biomation in Cupertino, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

Line Voltage: The Model 851-D may be operated from either 115 or 230 Vac (±10%) power lines. A rear panel line voltage switch permits quick and safe conversion for operation from either voltage.

CAUTION: Before plugging instrument into AC power line be sure line voltage switch is properly positioned.

Power Cable: The Model 851-D is equipped with a detachable 3-wire power cable. Proceed as follows for installation:

a) Connect line-cord plug (3-socket connector) to AC line jack at rear of instrument.

Power Cable (cont'd)

b) Connect plug (2-blade with round grounding pin) to 3-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only 2-blade outlet is available, use connector adapter, then connect short wire from side of adapter to ground.

2.5 Preparation for Use

The Model 851-D is not a "self-contained" instrument in that it must be interfaced with other types of instrumentation for the data to be visible or analyzed. The following sections of this manual cover operation, set ups, and interface requirements.

2.6 Initial Warm-Up

Although the Model 851-D is a solid state instrument, a brief warm-up period of approximately 5 min. is required for the input amplifiers and comparators to reach thermal stabilization. This warm-up period is recommended for both the Model 851-D and its associated output device.

SECTION III

PRINCIPLES OF OPERATION

3.1 Basic Functional Description

The Model 851-D offers convenient and useful capabilities for the analysis of digital signals. The unit is an eight-channel solid-state digital recorder, which operates at a maximum record rate of 50 MHz simultaneously for all eight channels. Figure 3.1 presents a block diagram of the 851-D.

The memory in the 851-D stores a 512-bit record for each of the eight channels. This memory "snapshot" may be taken in either of the following record modes: Pretrigger or Delayed mode. In the Pretrigger mode the recording process begins upon activation of ARM switch or Remote Arm input. The unit continuously monitors and records the status of the eight input lines at the selected clock rate. When a trigger event occurs, recording is terminated (or continued until the selected trigger delay has elapsed). Selection of the delay determines the position of the "snapshot" before and after the trigger event. In the Delayed mode the recording process begins at the (delayed) trigger event. This means that the "snapshot" may be delayed downstream from the trigger event at a selectable number of sample intervals (0 to 9999). Therefore, eight points in a digital circuit can be continuously monitored, waiting for a specific fault or logic event. When the event occurs, a contiguous record of events before and after (Pretrigger mode) or a delayed recording (Delayed mode) is made for display and subsequent analysis.

3.11 Input Threshold

The definition of a stored data signal as a binary "1" or "0" is determined by switch-selected logic threshold levels. Channels 1-4 are independently selectable from Channels 5-8. Six standard threshold levels are available on each of these two switches as well as independent, contiguously variable controls. Standard threshold selections are TTL, ECL, MST, +2.0, +2.5 and -2.5. The VAR position controls provide +2.4 V continuously variable for both the input threshold level selections. In addition, selection of X1 or X10 probe input selection provides full threshold sensitivity for X10 attenuated, higher bandwidth probes.

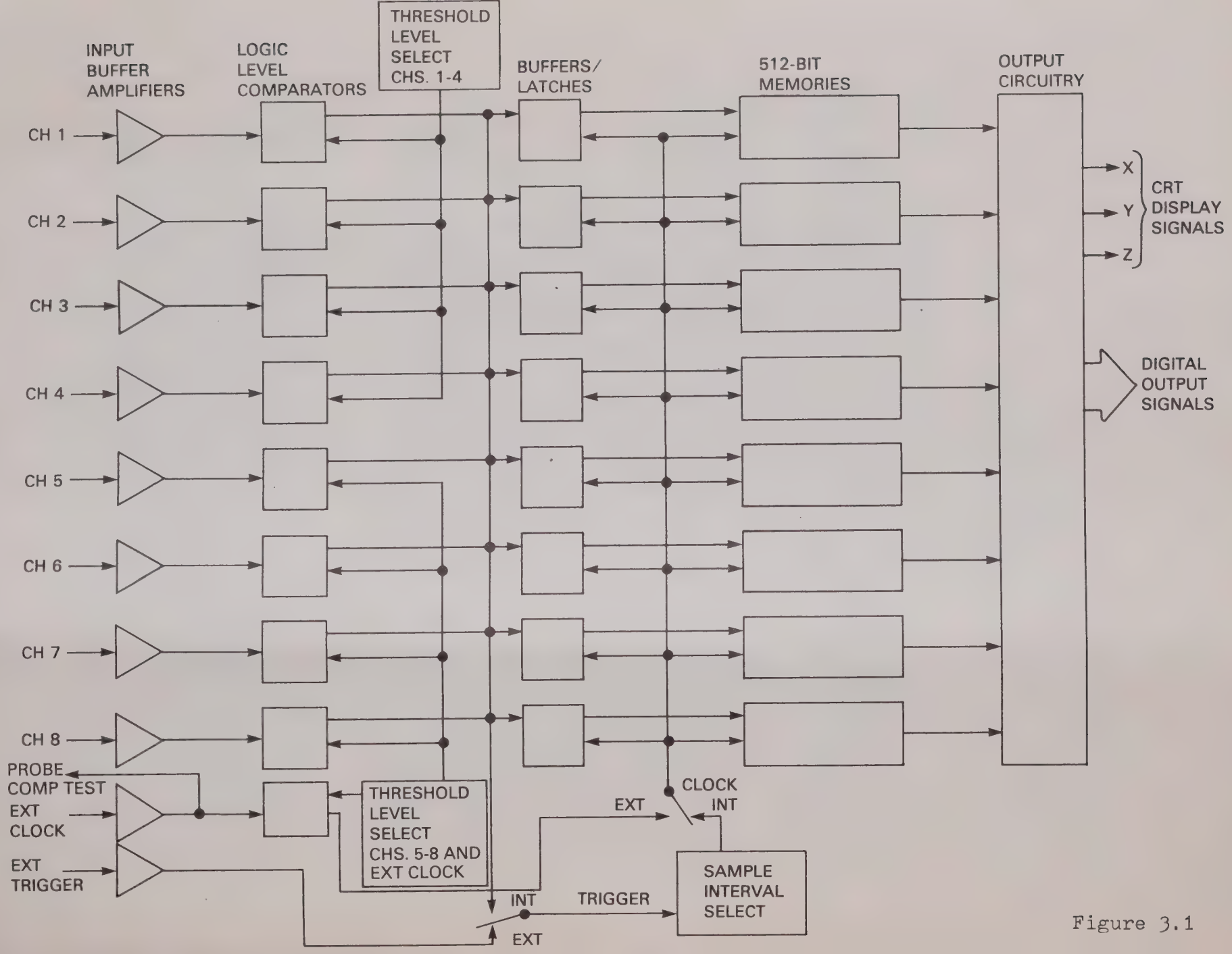

INPUT BUFFER AMPLIFIERS
LOGIC LEVEL COMPARATORS
THRESHOLD LEVEL SELECT CHS. 1-4
BUFFERS/ LATCHES
512-BIT MEMORIES
OUTPUT CIRCUITRY
CH 1
CH 2
CH 3
CH 4
CH 5
CH 6
CH 7
CH 8
X
Y
Z
CRT DISPLAY SIGNALS
DIGITAL OUTPUT SIGNALS
PROBE COMP TEST
EXT CLOCK
EXT TRIGGER
THRESHOLD LEVEL SELECT CHS. 5-8 AND EXT CLOCK
CLOCK
EXT
INT
SAMPLE INTERVAL SELECT
INT
TRIGGER
EXT

Figure 3.1

3.12 Sample Mode

In the "SAMPLE" mode of operation, the input levels are strobed into the memory as "1" or "0" based on the signal level with respect to the selected threshold at the time of the active edge of the clock.

3.13 Latch Mode

The "LATCH" mode of recording permits narrow spikes to be recorded. Any spike (positive or negative) with sufficient amplitude and duration causes an input latch to set. This changes the state of the next bit to be written in memory. In this way, narrow spikes or "glitches" occurring at random times between sample clock transitions can be captured.

Typically, a glitch that exceeds the threshold by 250 mV threshold overdrive can be as short as 5 nsec and still be detected. See Figure 3.2.

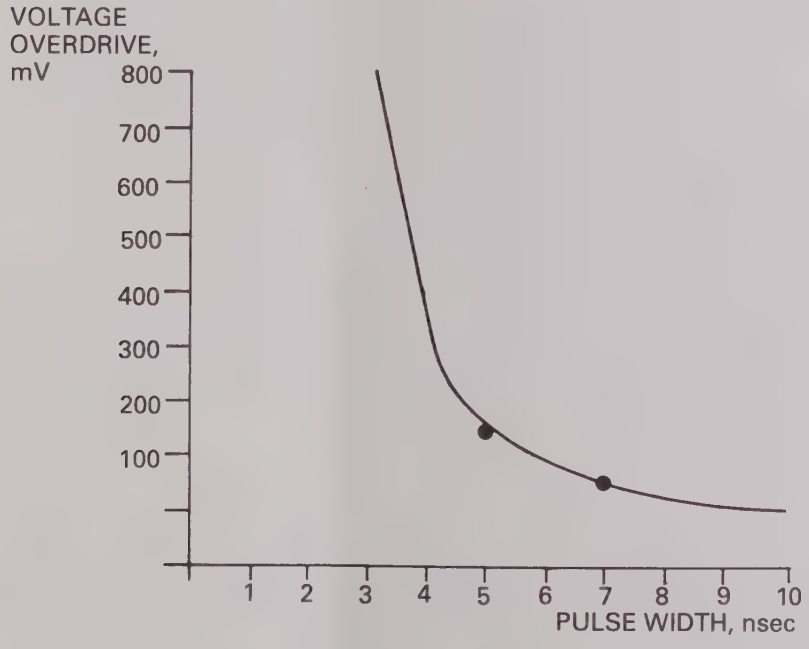


Figure 3.2
Relationship between voltage over threshold and pulse width of glitch that can be typically latched in the LATCH mode of operation.

3.14 Signal Inputs

The eight signal inputs and the clock input all have an input impedance of 1 MΩ, 10 pF.

3.15 Record Rates

The internal clock interval is switch selectable from 20 msec to 0.02 μsec, in a 1-2-5 sequence. The clock of the device or system under test may be input via the front panel to effect synchronous recording, a distinct advantage when

synchronous logic is being examined. The external clock logic threshold is set by the Channel 5-8 threshold selector switch. Falling or rising clocking edge is also selectable.

3.16 Delayed Record Mode

A Delayed record sequence is started by the Trigger function and stops after the entire memory has been refreshed. The trigger function can be derived from a parallel combination of input signals, true or false from an external source, or manually. The trigger can also be delayed by as much as 9,999 clock intervals in single clock increments. This mode and the Pretrigger record mode are illustrated in Figure 3.3. In the Delayed mode a static delay of 4 sample intervals exist from the trigger event until data is stored in the memory of the 851-D. The Pretrigger mode must be used to observe the trigger event and the three samples directly following that event.

3.17 Pretrigger Record Mode

The Pretrigger record mode is unique and very useful. With the Pretrigger mode selected, the unit begins recording upon receipt of the Arm command, and continuously updates the memory with new data (destroying the "oldest" data) much like recording with a tape loop. The amount of trigger delay selected determines the amount of prior-trigger data stored when recording ceases; e.g., selection of a 250 clock interval trigger delay will cause the unit to continue recording for 262 clocks after the trigger, and then cease recording, while retaining 250 words of contiguous prior trigger data. In this way, eight points in a digital circuit can be continuously monitored, waiting for a specific fault or logic event to trigger the unit. When the trigger occurs and the delay is counted out, a contiguous record of events (before and after the trigger) is recorded and displayed.

3.2 Recording Considerations

Because the Model 851-D can record as a function of either the internal clock or an external clock, note should be taken of some basic differences in these two methods.

When the internal clock is used for recording, no particular phase relationship will exist between this clock and any synchronous information rate in the signals being recorded. Therefore, a beat frequency can exist between these two basic rates. If the 851-D internal clock is at least 10 times higher in frequency than the signal rate, very little effect will be noted in the recorded data. For high signal rates (with respect to the record clock), a beat rate effect can be seen by varying widths in the recorded "pulses" and even periodic "dropped" bits will be observed when these rates approach the limiting ratio of two to one.

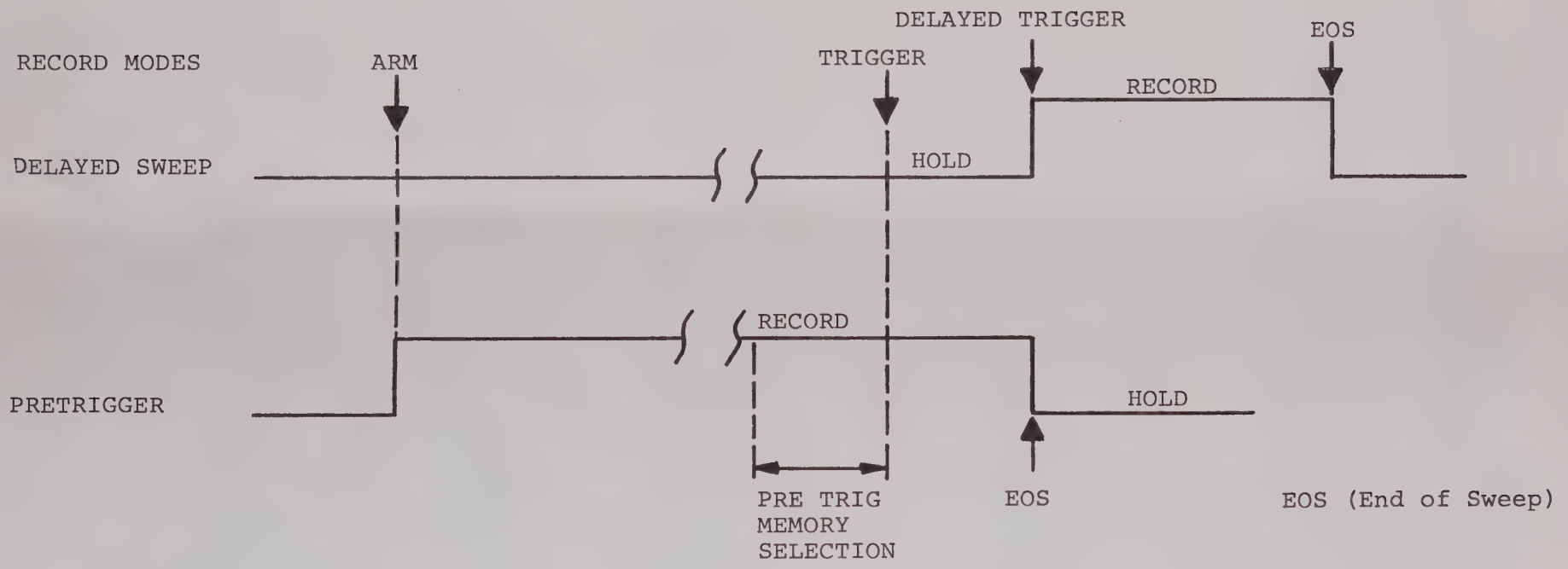


Figure 3.3 Model 851-D Recording Control Functions

When the synchronous clock used for the generation of the input signals to the 851-D is used as the record clock in the 851-D, no phase errors exist and no beat frequencies will be evident; i.e., the beat note is zero frequency. In this case, signals with information rates up to and including 1/2 the clock frequency can be recorded without distortion. This is called synchronous recording. The fixed delay between input data signals and the external clock input at the threshold detectors is typically 13 nsec. See Figure 3.4.

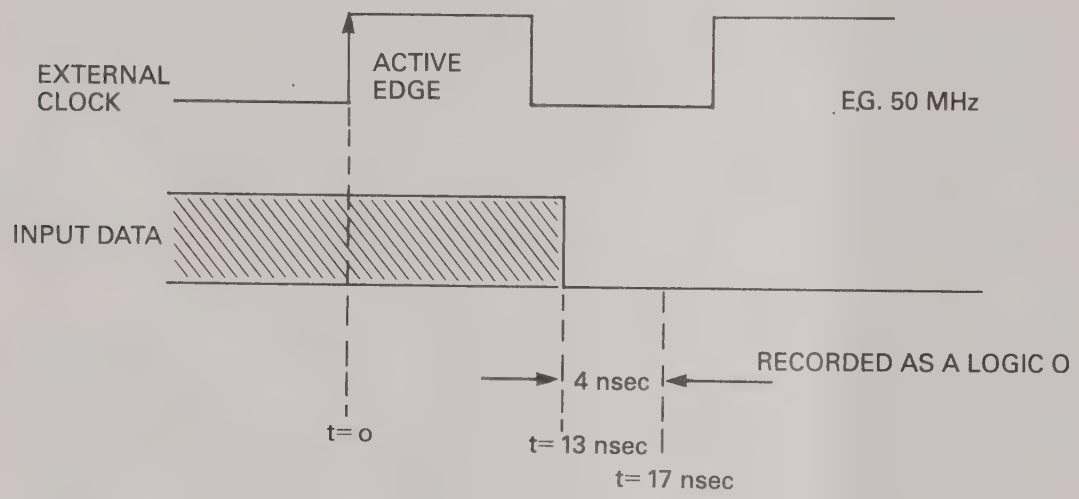


Figure 3.4

Sample mode timing requirement. When using an external clock, data may change states anytime up to typically 13 nsec after the active edge of the clock. Once the logic state change is made, it must be maintained until 17 nsec after the active clock edge to be recorded in that state.

Bear in mind that the 851-D is an instrument for the detection and storage of digital data. As such, the unit only discriminates between two different levels as defined by the threshold switches. The data stored and displayed is NOT an analog representation of the input signals, but a pattern of "ones" and "zeros" that represent threshold crossings.

3.3 Outputs and Control Inputs

3.31 Display Output

Once Record is terminated, the unit automatically goes into a display mode where the contents are repetitively output to a CRT or triggered scope.

The display presentation is in an eight-trace timing diagram format. With no horizontal expansion, 500 bits of information per line are displayed, 50 per division. The 851-D has a movable display cursor. This cursor may be used to chose the point of display expansion. Display expansion may be selected in a mixed mode or in full expansion. In the mixed expansion setting, the display appears as X1 expansion to the left of the movable cursor and X5, X10, or X20 selectable to the right of the cursor. Full expansion provides 100 bits per line in X5, 50 bits per line in X10, and 25 bits per line in X20 expansion.

3.32 Digital I/O

The digital data in the Model 851-D's memory can be output under the direction of two digital control inputs via the rear panel, 24-pin digital interface connector. These inputs are the OUTPUT REQUEST line and the COMMAND line. Once digital output has been requested the 851-D loads an 8-bit parallel word on the output buffers, signaling the receiving device with a FLAG output signal. These 8 bits are the first bits of each of the 8 input signals. Successive words may be strobed onto the output buffers by the COMMAND input up to a maximum strobe rate of 30 kHz. All Data outputs are TTL levels, positive true. Other input control lines, as well as output status signals, are available at this connector. See Section V for complete details.

3.33 Multi-Unit Synchronization

Several 851-D Logic Analyzers may be synchronized for extended recording length or increased parallel channel capability. This is done by simply interconnecting the Arm, Trigger, and Time Base I/O BNC connectors on the rear panel of each unit.

3.4 Operational Functions

The operation of the Model 851-D is basically concerned with the signals or events that determine the initiation and termination of the sampling and recording of the input signals and events, and their interrelationships in the functional operation of the unit.

3.41 Sweep and Sweep Time

In the following discussions the terms "sweep" and "sweep time" are often used. The term "sweep" is used to designate the succession of samples taken on the input signals during a recording sequence. The term "sweep time" is used to designate the amount of time required to fill the memory with contiguous samples of the input signal. When this term is used, it is normally assumed that the entire sweep was accomplished at a single linear sample rate.

3.42 Arm, Trigger, and End of Sweep Function

The Arm, Trigger, and End of Sweep (EOS) functions, together with adjustable delay (associated with the Trigger event), control the sequence of events in the operation of the record cycle of the Model 851-D. The effect of each of these functions or events on the sequence of events is dependent upon the mode of operation selected for the unit. This interdependence will be described below.

In all recording modes, an Arm function must precede a Trigger function. The unit cannot be triggered before it is armed. The Arm function may be initiated manually via front panel pushbutton or externally via rear panel input. Once the unit has been armed, it can accept a trigger.

The Trigger function may also be initiated in the same manner as the Arm function. In addition, the unit may detect a Trigger from any one channel, or via the coincidence of a parallel combination of bits as selected on the front panel. Furthermore, the combinational trigger selection allows the 851-D to trigger when the selected parallel combination becomes true with the inputs or, when it no longer coincides with the selections, becomes false.

3.43 Modes of Operation

The operational modes for the record sequence in the Model 851-D are determined by the record mode selected. Three record modes are provided. They are Pretrigger, Delayed Manual, and Delayed Auto. The Delayed modes are identical in operation except for derivation of the Arm signal. In the Delayed Auto mode the Arm signal occurs automatically after a record sweep and one complete display output sweep. In the Delayed Manual the Arm signal must be provided by activation of the front panel switch or an external signal input to the rear panel. For purposes of further discussion, Delayed Auto and Delayed Manual will be treated as Delayed Record Mode. See Figure 3.3 for an illustrative reference.

3.431 Delayed Record Mode

In the Delayed record mode, the record cycle is initiated by the (delayed) Trigger, and is ended at the End of Sweep (EOS), at which time all 512 bits/channel of the memory have been loaded with new data. In the Delayed mode, there exists a four-sample delay between the start of the record cycle and storage of data in the memory. This means that the 512 word "snapshot" is taken four clocks downstream from the (delayed) triggering event. This mode can be used in various ways depending on the setting of the Trigger delay. With the delay set to zero, recording begins at the trigger event and ends 516 clock intervals later. With a delay set into the Trigger delay selector, recording is held off until after receipt of the trigger and timing out of the trigger delay. When the delay has elapsed the recording process begins, ending again after 516 clock cycles.

The delayed sweep mode of operation is used in situations where the only good trigger signal precedes the data to be recorded. In many cases the delay between the Trigger and the desired information is greater than the optimum sweep time. In these cases the signal would not be recorded with sufficient resolution to be useful. By delaying the initiation of the sweep with the Trigger delay and sampling the signal at a faster rate, the information can be recorded with good time resolution.

3.432 Pretrigger Mode

Pretrigger recording is a unique feature of Biomation Recorders. Pretrigger recording allows the capture or recording of signals that are not known to be significant for recording until after the signal has occurred. Another good use of this mode is in cases where the only good Trigger available follows the information of interest.

In the Delayed record mode the starting point for filling the memory with new information is when the Trigger occurs, or later. In the Pretrigger record mode of operation the memory is continuously being updated after the unit has been Armed, and will discard information (from the "other end" of the memory) at the same rate. When a trigger event occurs, the 851-D saves the selected Pretrigger portion of memory and continues recording until the remaining portion is filled with data occurring after the trigger event. If the PRE-TRIG memory switches have been set to 100 bits, the memory will contain 8 X 100 bits of pretrigger and 8 X 412 bits of data recorded after the trigger.

SECTION IV

OPERATION

4.1 Introduction

This section identifies and describes front panel controls, rear panel connections, and typical operating procedures. Included are complete descriptions of front panel controls and their effective ranges, location and proper use of rear panel connectors, set up procedures prior to using the Model 851-D, and step by step operating procedures for various modes of operation. A thorough understanding of this section is essential to the successful use of the instrument.

4.2 Front Panel Controls and Connectors

4.21 Control Clusters

The controls of the Model 851-D may be divided into five groups. Each group contains separate controls with related functions. Figure 4.1 is a front panel photograph of the 851-D. The five control groups are as follows:

Record Mode and Trigger

Input Mode and Thresholds

Clock

Display

General

4.22 Record Mode and Trigger

(1) RECORD MODE. In the PRE-TRIG position, the unit fills the memory with new data when the front panel MANUAL ARM switch or remote Arm inputs on the rear panel are activated. Recording continues, dumping the oldest data off the end of the memory until the trigger event occurs. At that time the portion of the memory selected (PRE-TRIG MEMORY (2)) is saved. The remaining portion of the memory is filled with new data contiguous to the trigger event.

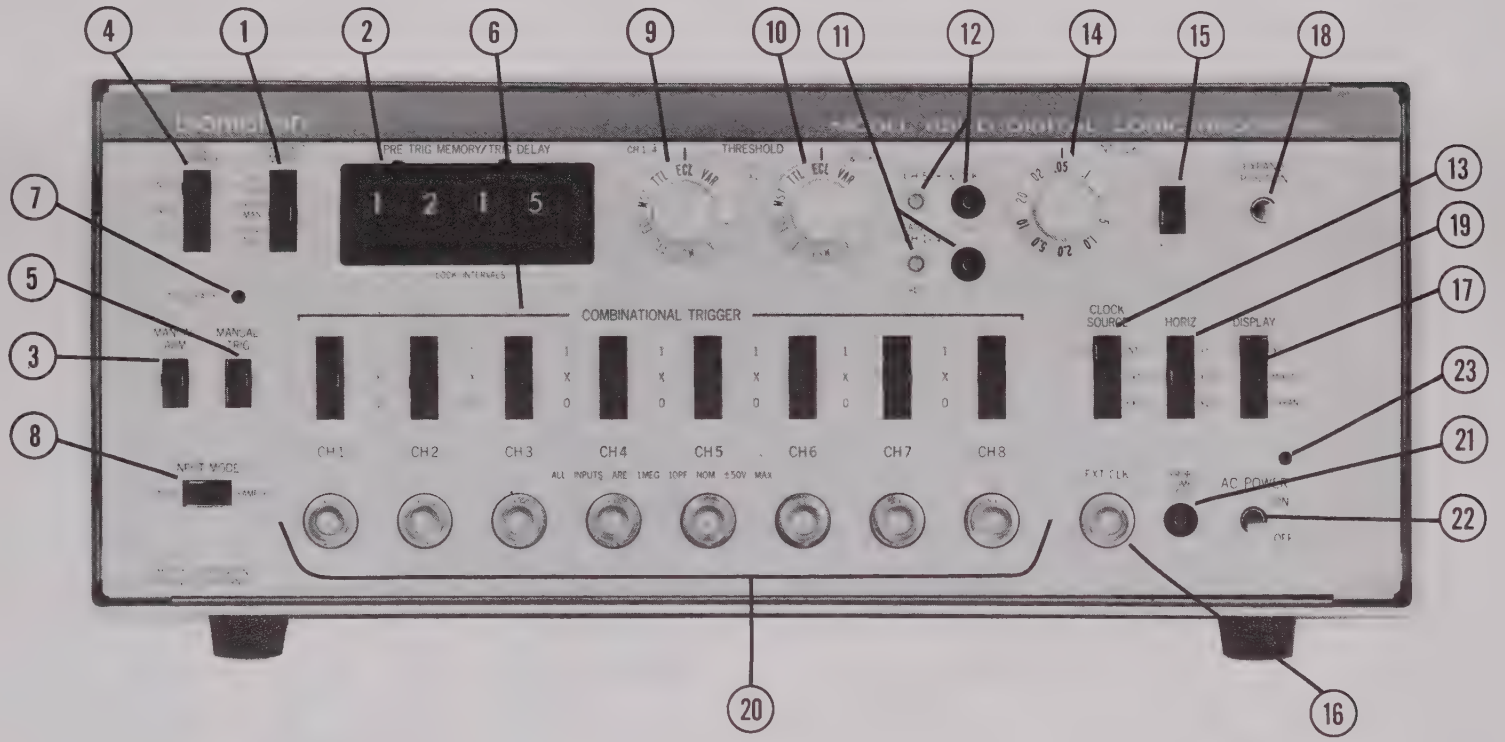


Figure 4.1 851-D Front Panel

In the DELAY MAN mode, an Arm initialization alerts the 851-D that it may accept the next designated trigger event. When that event occurs, the TRIG DELAY starts. When the selected trigger delay has elapsed (0 to 9999 clock intervals), the memory begins to fill with new data continuing until 512 bits/channel have been recorded.

In the DELAY AUTO mode, the Arm function is activated by the 851-D internally. Recording is accomplished exactly as is done in the DELAY MAN mode. Once the 851-D has completed a single display output sweep (requiring 16 msec), the unit automatically re-arms itself and will accept the next designated trigger event. This mode of recording is very convenient for initial set-up because no manual or external Arm input signal is required for acceptance of a trigger event.

(2) PRE TRIG MEMORY/TRIG DELAY. In the PRE TRIG RECORD MODE (1), these convenient digiswitches allocate the portion of the Model 851-D's memory that is saved for prior trigger information. Note that the memory displayed is 500 bits/channel long. Setting these switches to 500, therefore, will place the trigger event at the end of the display memory. The 499 bits/channel displayed to the left of this trigger location were recorded prior to the trigger, thereby giving a look back in time from a trigger event. Attention should be paid to the amount of time between initialization of the Arm function and recognition of the Trigger event. If after arming the 851-D only a 100-clock interval period elapsed before the trigger event was recognized with the PRE TRIG MEMORY selection set to 500, the unit would not have had sufficient time to record all 500 pretrigger samples. Therefore, 400 samples/channel would be left in the memory from a previous recording.

The memory is 512 bits/channel long. The first 500 bits/channel are specified to be valid data samples. The display output sweep consists of only these 500 bits/channel.

CAUTION: Setting the PRE-TRIG MEMORY to greater than 500 samples is an illegal mode for the Model 851-D.

In the DELAY MAN or DELAY AUTO modes, the PRE TRIG MEMORY/TRIG DELAY designates the amount of delay that elapses prior to the record start. When a trigger event is recognized by the Model 851-D, the beginning of the record cycle may be postponed from 0 to 9999 clock intervals. The inherent static causes the stored data to lag this delay setting by 4 sample intervals.

(3) MANUAL ARM. Pressing this momentary switch starts the unit recording when the RECORD MODE switch (1) is set to PRE TRIG. In DELAY MAN mode it alerts the 851-D to accept the next trigger event. When recording in the pretrigger mode, the entire memory may be set to all "zeros" (low) by holding the Arm switch down for a minimum of one single sweep (500 X sample interval).

(4) TRIG SOURCE. Selects origin of the trigger event. INT(T) causes the unit to continuously monitor the 8 input signals upon activation of the Arm function when the inputs coincide (become true) with the COMBINATIONAL TRIGGER (6) selection, a trigger pulse is generated. See Figure 4.2.

In the INT(F) Source, the 851-D observes the input channels waiting until the input combination no longer coincides with the trigger selection. In other words, the input signal combination becomes "false" with respect to the trigger combination switches.

In the EXT source, the unit looks for a trigger pulse (ECL level or TTL level) from the rear panel BNC TRIG IN or I/O connector, respectively.

(5) MANUAL TRIG. Pressing the Manual trigger momentary switch provides an overriding trigger pulse to the 851-D in any TRIG SOURCE (4) selection. The unit will only recognize this trigger, of course, once the Arm is activated.

(6) COMBINATIONAL TRIGGER. These switches may be used to select any one or a combination of channels as a trigger source. The 8 switches have three positions: "1" (high), "X" (Don't Care), and "0" (low).

(7) TRIGGER READY. This light indicates that the Model 851-D is armed and is waiting for the defined trigger event.

4.23 Input Mode and Thresholds

(8) SAMPLE/LATCH. In SAMPLE position, the unit compares input levels with the preselected threshold level and stores a high or low, as appropriate, on the positive transition of the clock. Thus, the data stored in memory reflects the input states at the clock transition.

In the LATCH mode, the unit stores as above for single threshold transitions in a clock period, but also "latches" to a state opposite that last stored when multiple transitions occur in a clock period. For instance, a single narrow pulse between clock transition would not affect the memory contents in SAMPLE mode but would affect the stored data in LATCH mode. This "glitch" catching feature works for either positive or negative pulses by "stretching" the random pulse to one full data period. The 851-D will typically "latch" on pulses as narrow as 5 nsec. See Figure 4.3.

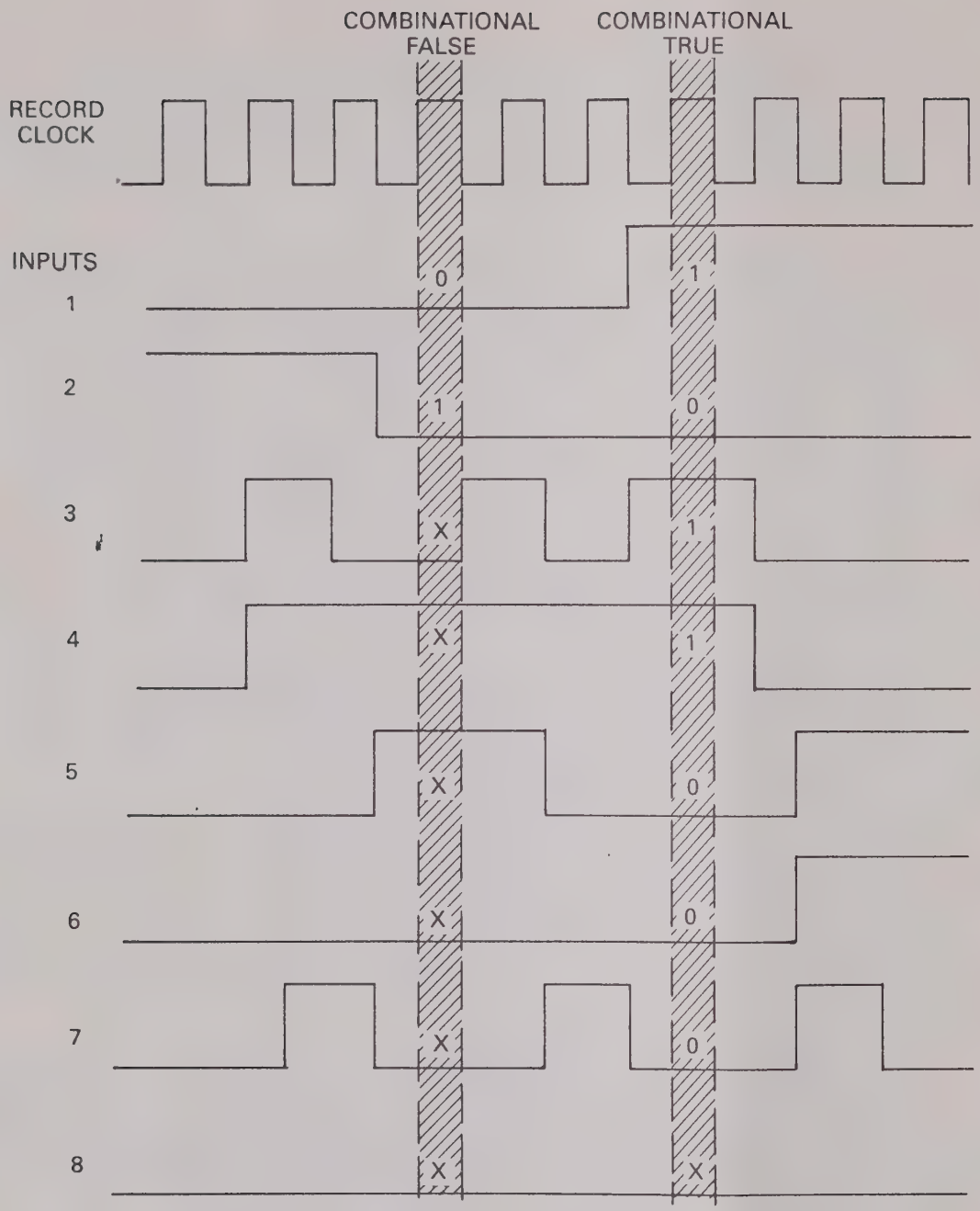


Figure 4.2. This diagram illustrates an example of conditions for combinational true and combinational false triggering. Notice that the CMBL (F) trigger condition occurs during the clock cycle for which the combination of inputs no longer coincides with the trigger combinations selected.

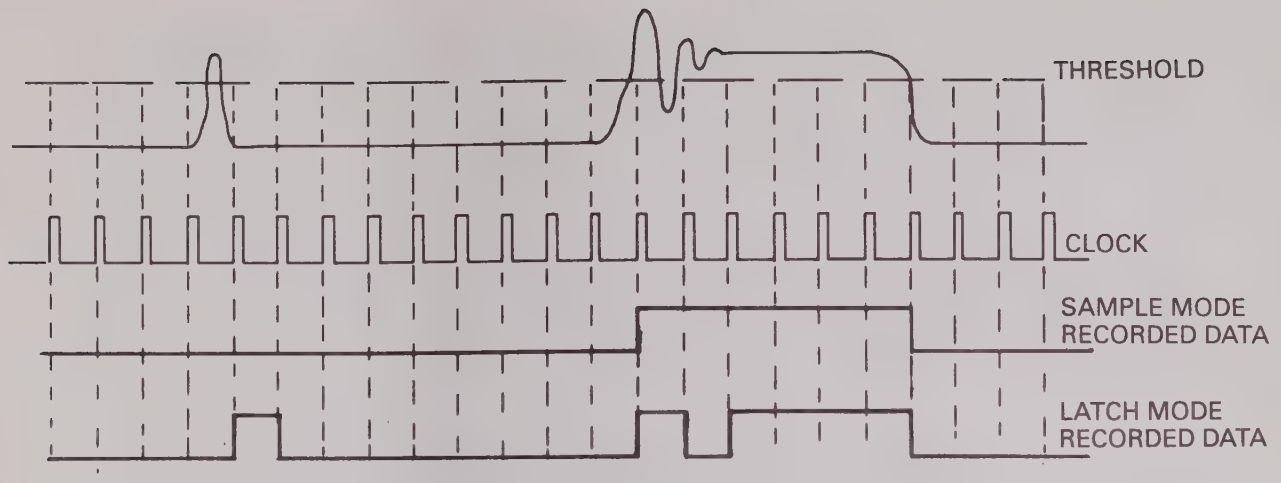


Figure 4.3

This diagram illustrates two ways in which the LATCH mode of recording can provide valuable information about the circuit signal that cannot be positively captured with the SAMPLE mode of recording.

(9), (10) THRESHOLD VOLTS. Provides switch selection of MST (0.0 V), TTL (1.4 V), ECL (-1.3 V), A (+0.25 V), B (-0.25 V), and C (+0.20 V) thresholds, as well as (VAR). These two switches are set independently for Channels 1-4 and 5-8. The black nomenclature is for use with unattenuated (X1) probes; red nomenclature is for use with X10 attenuated probes. In the VAR position, the user may adjust the vernier threshold settings using the potentiometer marked CH 1-4 ADJ for Channels 1 through 4, and the potentiometer marked CH 5-8 ADJ for Channels 5 through 8. A test point is provided to the right of each potentiometer for observation of each setting.

When the input level is more positive than the threshold, a logic "one" (high) is stored in memory; when the input is less positive, a logic "zero" (low) is stored.

(11), (12) VARIABLE TEST. To set a vernier threshold, set THRESHOLD (CH 1-4 and/or CH 5-8) to VAR. Adjust CH 1-4 and/or CH 5-8 potentiometer with a screwdriver for the desired threshold as measured at the test points, adjustable $\pm$2.4 V. The output impedance at this test point is 10 kΩ. The accuracy of the threshold voltages are nominally $\pm$5% of maximum threshold readings.

4.24 Clock

(13) CLOCK SOURCE. Selects internal (INT), external rising edge (EXT $\int$), or external falling edge (EXT λ) clock source. With (INT) selected, the INT CLK (14) switch is used to provide the sample rate for strobing the input data signals. (EXT $\int$) or (EXT λ) activates the EXT CLK BNC connector (16). The unit will not record until an external clocking signal is provided.

(14) INT CLK. Selects, in conjunction with the μsec/msec switch (15), the choice of internal clock intervals of 0.02,

0.05, 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, 10.0 and 20.0 µsec/msec clock input.

(15) µSEC/mSEC. Provides multiplication factor for switch (14).

(16) EXT CLK. This BNC connector allows input of an external clock when switch (13) is either in the EXT ∫ or EXT ⌇ position. Input impedance 1 MΩ. Clock threshold set by CH 5-8 voltage threshold switch (10).

4.25 Display

(17) DISPLAY. The display defines the horizontal expansion mode to be used. The (X1) position display output consists of the 8-line timing diagram of 500 bits per line. A more detailed view of any portion of this display may be obtained by moving the vertical line cursor to the point of interest using the EXPAND POSITION (18) control, selecting (MIXED) or (EXPAND) positions.

The (MIXED) position provides X1 horizontal expansion to the left of the movable cursor and X5, X10, or X20 horizontal expansion, as selected on the HORZ switch (19), to the right of the cursor. This mixed mode of expansion allows the user to view data leading up to the point of interest as well as detailed expansion of data to the right of that point.

The (EXPAND) position horizontally expands the timing diagram to X5, X10, or X20 as selected on the HORZ switch (19). The segment viewed on the display begins from the vertical cursor location and contains 100, 50, or 25 bits per line, respectively, with the expansion factor selected. Movement of the EXPAND POSITION control (18) selects the memory location from which the expansion begins.

(18) EXPAND POSITION. This control, when used in conjunction with the DISPLAY switch (17), determines the point of horizontal display expansion. With the DISPLAY switch set in the (X1) position, the expansion control is used to locate the vertical cursor on the time diagram display. The control has two speeds, as well as left and right direction control. Movement of the control stick to the right or left produces a corresponding one-bit horizontal movement of the display cursor. If the control stick is held over for one second, then the cursor will resume movement at a constant rate until the control is released.

The cursor remains visible with DISPLAY (17) set to (MIXED). Data to the left of the cursor remains at X1 expansion while data to the right is expanded to the HORZ (19) switch selection of X5, X10, or X20. Movement of the EXPAND POSITION control changes the memory location at which this mixed expansion starts.

In DISPLAY (17) (EXPAND) position, the display is comprised of 100, 50, or 25 bits/line of data determined by the HORZ switch (19) location. This window of data begins at the signal location where the cursor is positioned. Movement of the EXPAND control slides the cursor, thereby moving the expansion window along the timing diagram.

(19) HORZ. This switch selects the X5, X10, and X20 expansion factor for mixed and full expansion operation of the display output. In full expansion, DISPLAY switch (17) set to (EXPAND), X5 provides a 100 bits/line window of the timing diagram starting at the display cursor location. X10 provides a 50 bits/line window, and X20 provides a 25 bits/line window. At X20, 2.5 bits or samples of the recorded signal per division appear on the CRT or oscilloscope. At the highest recording rate, 50 MHz (20 nsec/sample) in X20 expansion, the time resolution is 50 nsec/division on the CRT.

4.26 General

(20) CH 1 THROUGH CH 8. 8 BNC connectors for input of as many digital signals. Input impedance is 1 MΩ, 10 pF to ground.

(21) PROB COMP TEST. This probe compensation test point is a direct connection to the EXT CLK input buffer amplifier. Allows user to compensate his probes with respect to the input circuitry of the 851-D.

The probe to be compensated is connected to EXT CLK, and to a square wave generator. A properly compensated scope probe, connected to an oscilloscope, is placed on the COMP TEST point. The probe at EXT CLK is then adjusted until the square wave on the scope is normal. The 851-D MUST be powered up to perform this adjustment.

Each of the eight probes to be used with the 851-D may be compensated in this manner. However, each probe must be connected in turn to the EXT CLK input.

(22) AC POWER. When switch is ON, LED (23) lights indicate power has been applied to the 851-D.

4.3 Rear Panel Connectors (See Figure 4.4)

(1) X Output. Repetitive 1 V p-p ramp waveform, with a period of 2 msec. Adjustable 0.7 V to 2.5 V internally.

(2) Y Output. Repetitive 2 msec stair step ramp, each step equally spaced in amplitude. Data for each channel modulates each respective step level. Full range nominally 0 to 0.8 V. Adjustable 0.75 V to 1.25 V internally.

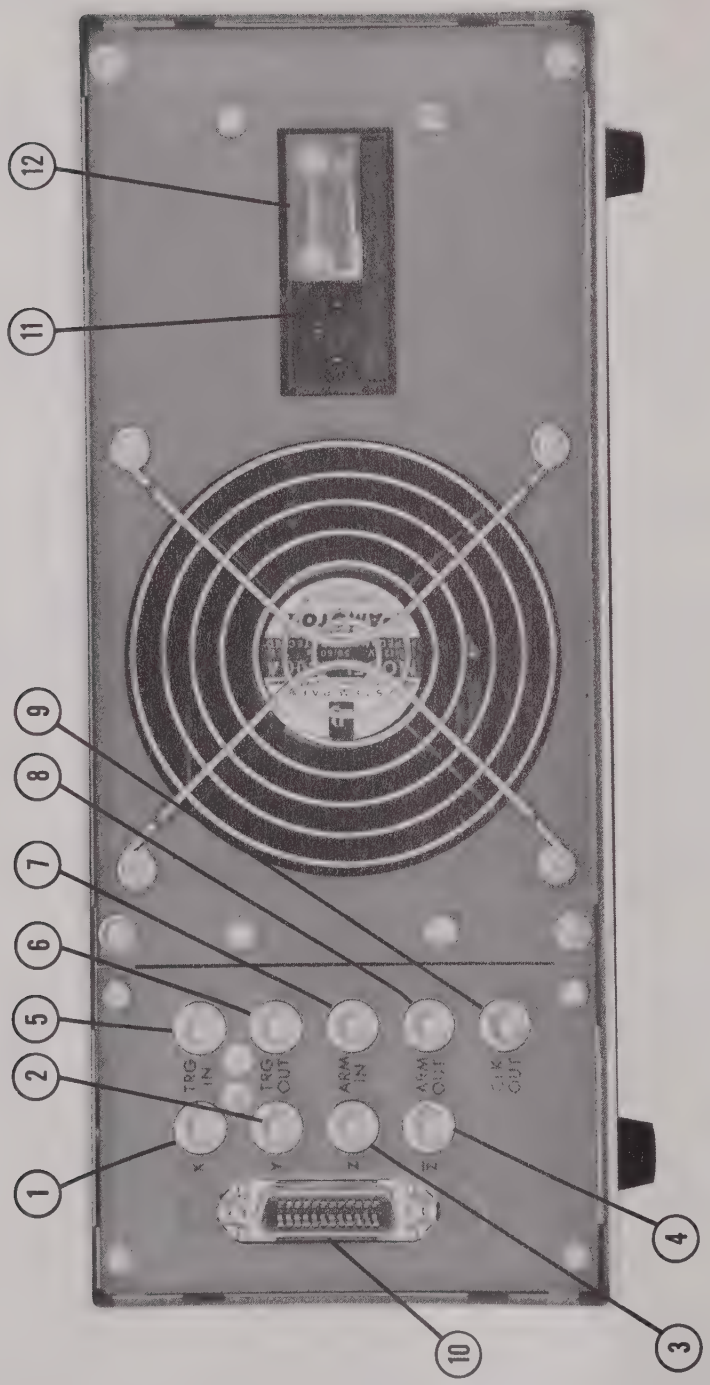


Figure 4.4 851-D Rear Panel

(3), (4) Z and $\overline{Z}$ Output. Z output nominally zero to +5 V pulse, 1 msec in duration and synchronized with the X output ramp for CRT retrace blanking. $\overline{Z}$ output inverted pulse of +5 V to zero.

(5) TRIG IN. Used in conjunction with connectors (6), (7), (8), and (9) for synchronization of multiple units for increased input signal capacity. ECL termination. Also used for external trigger input.

(6) TRIG OUT. Output ECL level when the unit recognizes the defined trigger event. Used in conjunction with TRIG IN (5) for synchronization of multiple units for increased input signal capacity. The slaved unit's TRIG SOURCE must be set to EXT.

(7) ARM IN. Input ECL termination for external Arm input or synchronization of multiple units.

(8) ARM OUT. Output ECL level occurring upon activation of the front panel MANUAL ARM switch. Used for synchronization of multiple units.

(9) CLK OUT. Clock output ECL driver. Used for synchronization of multiple units to provide simultaneous recording of all input signals. Must be properly terminated with 50 Ω impedance.

(10) I/O Connector. 24-pin interface connector used for all I/O operations. For procedural detail and pinouts, see Section V. Mating connector Amphenol Micro Ribbon 57-40240.

(11) AC Input, Fuse, Line Voltage Selector. AC input contains a line interference filter. Fuse: use a 1 A Slow Blow for 115 V operation, and a 0.5 A Slow Blow for 230 V operation.

4.4 Set Up Procedure

4.41 Initial Set Up

This section describes the connection of a Model 851-D with a CRT display or oscilloscope and the steps to record and display a known signal.

Before connecting the unit to line power, check the voltage selector switch on the rear panel to ensure that it

is set to the proper line voltage and be sure that the correct size fuse (as printed on the rear panel) is installed.

Connect the Model 851-D to a pulse generator with a manual single-pulse capability and CRT display as shown in Figure 4.5a or 4.5b. Depending upon the particular CRT or oscilloscope being used, it may be necessary to use the $\overline{Z}$ output of the 851-D for the retrace blanking signal.

CAUTION: Some older "tube types" oscilloscopes have a high voltage on their Z axis inputs. THIS COULD DAMAGE THE Z OR $\overline{Z}$ OUTPUT OF THE 851-D. PLEASE CHECK BEFORE CONNECTING THE UNITS TOGETHER.

Set the units (where appropriate) as follows:

Vertical sensitivity	0.1 V/div. uncalibrated, DC coupled
Vertical position	Bottom of display
Horizontal sweep	0.1 msec/div., (Figure 4.5a)
Horizontal sensitivity	0.1 V/div., DC coupled (Figure 4.5b)
Trigger input	-, DC coupled, external (Figure 4.5a)
Pulse Generator	Single manual pulse, 2.5 µsec wide, 0 to +3 V pulses

Set the Model 851-D as follows:

MODE:	Sample
THRESHOLD:	TTL (1.4 V)
DISPLAY:	X1
INT. CLK.	0.1 µsec
RECORD MODE	PRE TRIG
TRIGGER:	
PRE TRIG MEMORY:	100
TRIG SOURCE:	Internal
COMBINATIONAL TRIG:	CH 8 "1", all others "X" DON'T CARE

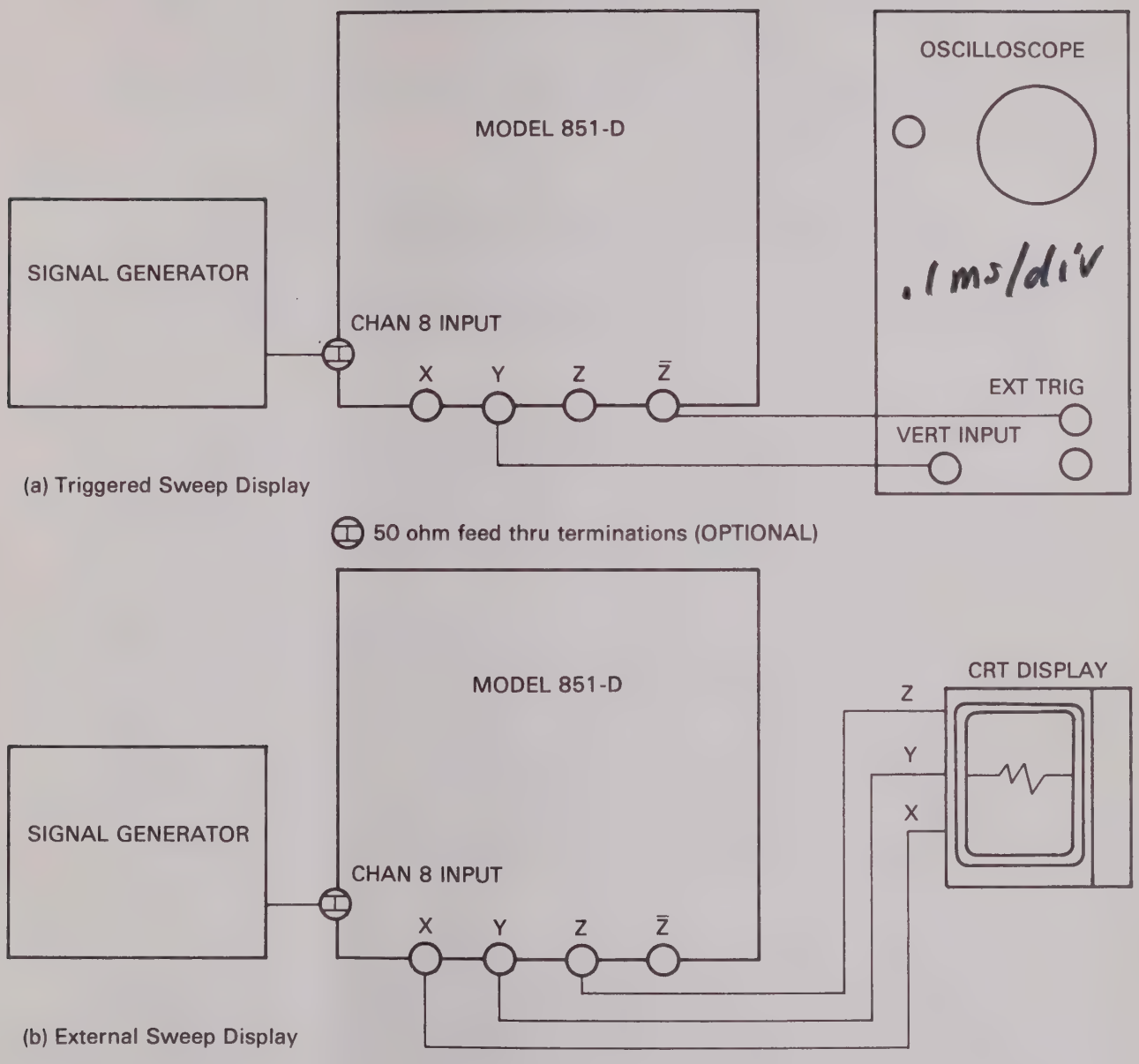


Figure 4.5 Display Interconnections

4.5 Operating Procedures

In this section two modes of operation will be discussed and illustrated. A pulse generator capable of generating a single pulse upon manual command is required.

Set the generator to give single, manually initiated pulses approximately 5.0 µsec wide, and 0 to +3 V amplitude.

4.51 Sample Mode

Press MANUAL ARM and pulse the generator. Figure 4.6 illustrates the display obtained. Channels 1 through 7 will display a low level, while Channel 8 displays the pulse. The pulse will occupy one division on the CRT, and be comprised of 50 clock intervals. One hundred clock intervals will have been recorded before the positive transition of the pulse.

4.52 Latch Mode

Set INT CLK to 50 µsec. In the SAMPLE MODE press the MANUAL ARM and pulse the generator while watching the display. The 851-D will trigger only if the leading edge of the internal clock coincides with the high state of the pulse. With a 50 µsec clock and a 5 µsec pulse it can be expected to take as many as 10 repetitions of the pulser for this coincidence to occur.

Now select the LATCH mode. Repeat pressing the MANUAL ARM and pulsing the generator. Observe that the unit captures the pulse each time and represents it with a one clock interval of 50 µsec. This is more readily observable by moving the cursor near the displayed pulse and expanding the time diagram with the HORZ-DISPLAY (EXPAND) switches. This feature is particularly useful for detecting narrow random noise pulses or "glitches". This mode operates in the same manner independent of the chosen clock interval. A glitch typically as short as 5 nsec may be detected and displayed at any clock interval.

4.53 Manual Trigger

To verify operation of each channel, change the pulse generator to a repetitive output, approximately 5 kHz rate, with the same pulse as before. Starting with Channel 1, connect the generator to the input BNC. Press the MANUAL ARM switch, and then the TRIGGER MANUAL switch. Several pulses of one clock interval will be displayed on the CRT, on the top trace. Repeat the above procedure for each channel, 1 through 7. The trace corresponding to that channel will display several pulses in turn. The 851-D should be in the Delayed Record mode with the trigger source set to EXT.

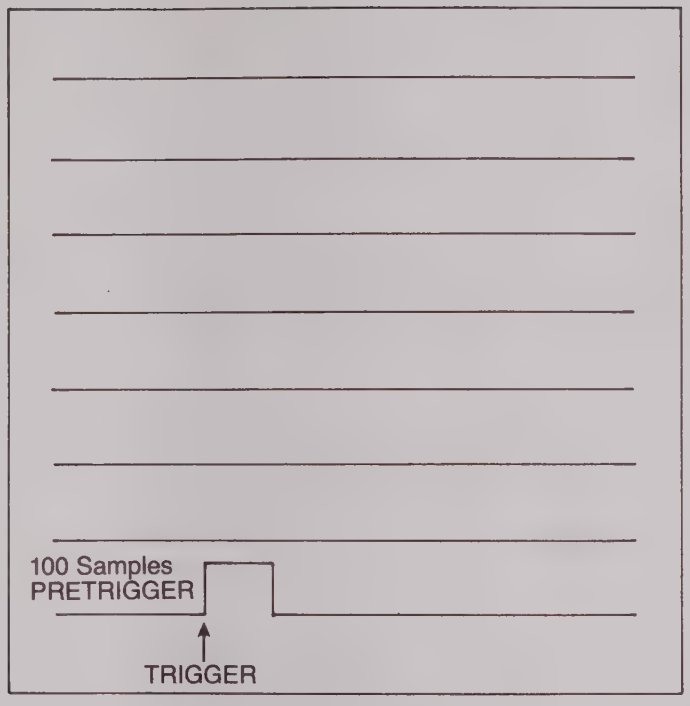


Figure 4.6 In the SAMPLE MODE, Channels 1 through 7 will display a low level, while Channel 8 displays the pulse.

SECTION V

OUTPUT INTERFACE

5.1 Introduction

The output interface of the Model 851-D includes two methods of analog output: one, using a CRT in an X-Y mode, and two, using an oscilloscope in the triggered mode. These methods are explained in Section 4.41.

The instrument also offers a digital output of data. This data is output in an 8-bit parallel format, the bits representing a simultaneous data entry for all channels. Five hundred twelve such 8-bit words are available through the digital output mode.

5.2 Digital Output

All inputs and outputs at the 24-pin rear panel connector are positive logic, TTL signals. Direct access to control gates is available at the connector. This connector provides the physical interface for digital data output. The connector is an Amphenol Micro Ribbon 57-30240. The mating connector is an Amphenol part number 57-40240.

The pin assignments, and signal descriptions for the digital interface are listed in the following table:

Pin #	Signal Name	Description
18	Data Output 1	These lines supply data stored in memory when the digital output procedure, outlined in Section 5.21 or 5.22, below, is followed. Buffering is provided.
19	Data Output 2	
16	Data Output 3	
17	Data Output 4	
22	Data Output 5	
23	Data Output 6	
24	Data Output 7	
21	Data Output 8 (OUTPUTS)	
2	Output Request (INPUT)	Line is normally pulled high. To initiate output, pull low to enable TTL level.

Pin #	Signal Name	Description
3	Command (INPUT)	Normally high. Changing to a low level causes unit to "fetch" next data word. The high to low transition time must be 200 nsec or less.
4	Auto Arm Mode (OUTPUT)	0 V when instrument is in Auto Arm, otherwise at -5.2 V (CMOS).
6	1 MHz Clock (OUTPUT)	TTL signal 0.8 µsec high, 0.2 µsec low.
14	Flag (OUTPUT)	Goes high when next data word is available, approximately 100 nsec after command goes low.
7	M>N ($\overline{\text{OUTPUT}}$)	Synchronous with display output. CMOS level, which is -5.2 V before cursor output address and 0 V after cursor address.
12	Record (OUTPUT)	Low when unit is recording; high otherwise.
9	-5.2 VDC	
8	+5 VDC	
11	Trigger (INPUT)	Logic Level Trigger input must be brought low to enable TTL level.
10	Remote Arm (INPUT)	Line is normally held high and brought low to arm unit.
1, 13	Ground	Power and logic return.

5.21 Digital Output Sequence - After Display

Immediately after recording, the 851-D will enter the display mode, repetitively cycling the memory and producing the X, Y, and Z display signals. In this condition, the Record (pin 12) output signal will be high. The Output Request (pin 2) input will be pulled high.

When a low is input to the Output Request, the Flag (pin 14) will go high, nominally 10 µsec later. Output Request should be held low until the desired memory transfer has been

completed. Output Request should then be returned high. When Flag goes high, the first data word in memory may be read on the data output pins 18, 19, 16, 17, 22, 23, 24, and 21. This first word will read all zeros. Upon receipt of the first COMMAND input, the second word of memory will be brought to the output buffers. All data from this second word to the 500th word are specified to be valid information. The first word and last 12 words are invalid.

The next, and subsequent data words will be presented on the data output lines after each Command (pin 3) input negative transition. For proper data output the interval between Command inputs should be no closer than 33 μsec giving asynchronous data word rates 30 kHz to DC.

5.22 Digital Output Sequence - After Record

If it is desired to output digital data immediately after Record, proceed as follows: Hold Output Request (pin 2) low. As soon as Record is complete (Record goes high), Flag (pin 14) will go high, indicating the first data word can be read. When this occurs, proceed with Command Flag operation as described above. When the desired memory length has been transferred, return the Output Request (pin 2) high for further record sweeps.

NOTE: The memory of the 851-D contains 8 X 512 bits. Only the second through 500th bits of each channel memory are specified to be valid digital output data.

CAUTION: If the ARM IN and/or TRIG IN BNC connectors on the rear panel are enabled, Remote Arm (pin 11) and Trigger (pin 10) must be left floating (high).

SECTION VI

CALIBRATION PROCEDURE

6.1 Calibration of Display Output

Adjustments are provided to calibrate the "X" and "Y" outputs of the 851-D to a specific output device. If accurate time measurements are to be made, the 851-D and the display device must be calibrated as a system. Before leaving the factory, the X and Y outputs are set at 1.0 V p-p (X1) and 0.8 V p-p respectively. Figure 6.1 shows the location of the adjustments on the control board for the X and Y levels.

Connect the 851-D to the Display as shown in Figure 4.5.

Turn on both instruments and allow them to warm up for at least 5 min., then proceed as follows:

1. Remove the top cover of the 851-D and locate the control board. This board is located on the right side of the unit. The appropriate adjustments are easily made from the top. Place the 851-D into TTL X1 threshold mode.

2. Locate the potentiometer marked "Y". Adjust "Y" so that each of the eight lines in the display mode are centered on each of eight divisions of the scope face.

3. Ensure that 851-D expansion is X1 and that the scope expansion is also X1. Locate the potentiometer labeled "X". Adjust "X" to give full-scale display in the horizontal direction.

The display adjustment is complete and the cover may now be replaced on the 851-D.

6.2 Recalibration of the Internal Circuits

The following calibration procedures are intended to be used in recalibrating the internal circuits of the 851-D. The entire instrument was calibrated before shipment and should not require any recalibration for at least six months or 1000 hours of operation.

6.3 Required Test Equipment

The following test equipment will be required to calibrate the Model 851-D:

1. Digital voltmeter, DC range 0-20 V minimum, 4 1/2 digit resolution minimum.

6.4 Power Supply Adjustment

Before recalibrating any circuit in the 851-D, it is necessary to check the power supply outputs to ensure proper levels. This is accomplished as follows:

1. Remove four screws in top cover.

2. Remove top cover.

3. Referring to Figure 6.1, front panel view, connect the voltmeter between the +5 TP and the ground TP. Voltage should be 5.00 ±0.02 V.

4. Readjust R37 on regulator board if required.

5. Connect the voltmeter to the -5.2 V TP. Voltage should be -5.20 ±0.02 V.

6. Readjust R49 on regulator board if required.

6.5 Channel 1-4 and 5-8 Threshold Adjustments

NOTE: Effective on serial #s of 6038 and above. Units with serial numbers below this do not have adjustable threshold levels.

Place voltmeter on 2 VDC scale, and set the displayed digits to 0000 with the highside connected to the low (guard) side. This adjustment is made by the offset adjust on most DVMs, or verify that the instrument used to set thresholds is good to three decimal places. The meter is in calibration on the 2 VDC scale and all threshold measurements are to be taken on this scale or erroneous data will occur. Repeat same procedure for any scale used during test.

Connect voltmeter between CH 1-4 test jack and chassis ground on front panel. Check levels as follows:

Threshold Control Position	Level at Test Jack
ECL (black)	-1.30 ±0.025 V
TTL (black)	+1.40 ±0.025 V
MST (black)	0.00 ±0.025 V
ECL (red)	-0.130 ±0.005 V

Threshold Control Position	Level at Test Jack	
TTL (red)	+0.140	±0.005 V
MST (red)	0.00	±0.005 V
A (red)	+0.250	±0.005 V
B (red)	-0.250	±0.005 V
C (red)	+0.200	±0.005 V

Readjust, using Figure 6.1 as a guide, any level that does not meet specification.

Repeat the previous step for channel 5-8 threshold level control and test point.

6.6 Input Offset Adjustments

Connect the DC voltmeter between pin 2 of channel 1 (AM685) L23 and ground. Voltage should record -0.012 V ± 0.002. If it is not, readjust R113 (10Ω Pot) until it does. Repeat this procedure for all eight channels and the EXT Clock input. To aid in finding all devices in each channel, use schematics and assembly drawings for main board in Section 9.

6.7 Input Capacitance

Connect a X10 scope probe from the scope calibration signal (a 1 kHz square wave with 5-10 V amplitude) to the EXT CLK input.

Connect a properly compensated probe from the scope channel 1 to the PROBE COMP test point. Gain of channel 1 will have to be set to 0.05 or 0.02 V/cm.

Adjust the calibration signal probe for minimum capacitance (i.e., for maximum overshoot observed on the scope.)

Adjust the input capacitance of the EXT CLK input to compensate properly the signal, i.e. square it up.

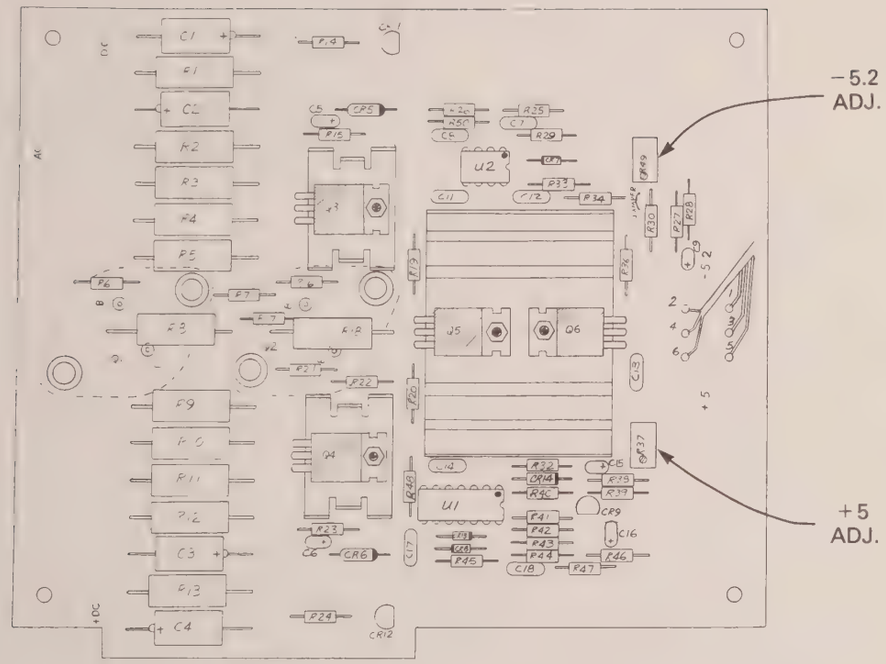
Do not change the setting of the scope probe adjustments for the remainder of this procedure.

Move the calibration signal probe to channel 8 and connect the scope input probe to observe the output of the channel 8 buffer (pin 2 of the 685).

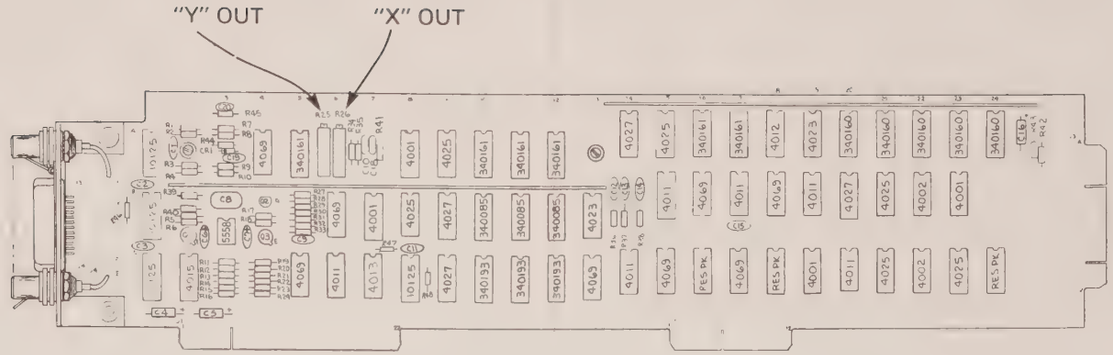
Adjust the input capacitance of channel 8.

Repeat for channel 7 - channel 1.

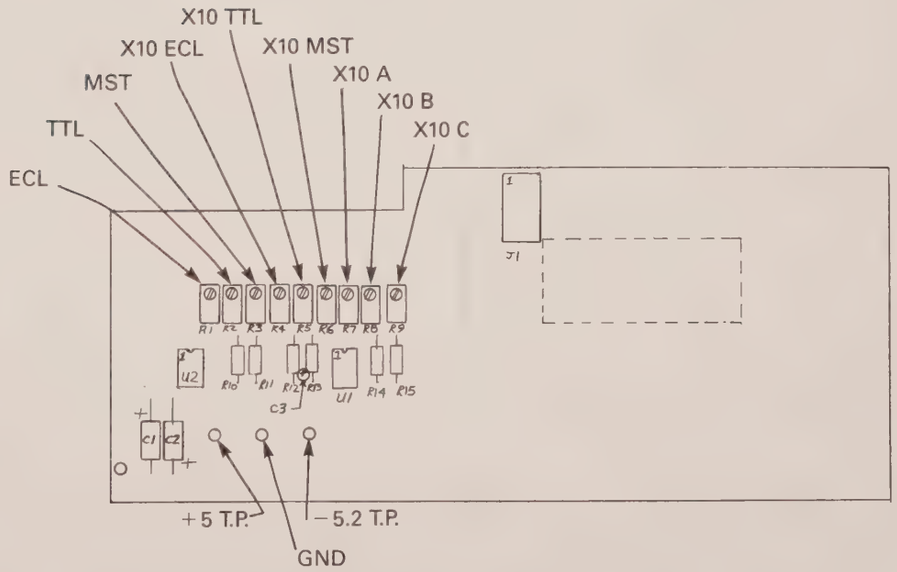
Replace top cover. This completes the recalibration of the internal circuits.



POWER SUPPLY
REGULATOR BOARD



CONTROL BOARD



DIGITSWITCH BOARD

THRESHOLD LEVEL
ADJUSTMENTS

Figure 6.1 Location of Adjustments

SECTION VII

TECHNICAL DESCRIPTION

7.1 General Description

The 851-D is divided into four subsystems:

1. Power Supply
2. Front Panel
3. Control Board
4. Main Board

The power supply operates from 110 or 220 V at 50 or 60 Hz and provides +5 V at 5 A and -5.2 V at 5 A. It also provides a fan for cooling.

The front panel has all of the operating controls and the circuitry for establishing the input threshold voltages.

The control board handles the display control logic and the low-speed timing generation.

The main board has the high-speed timing generation, the data input, the memory, and the Record control logic.

Figure 7.1A is a detailed functional block diagram. The front panel control lines are shown along the left side. The display outputs and the digital data interface outputs are shown along the right side. The block diagram is divided by a dotted line to indicate the division of the logic between the main board and the control board. The main board receives the data and processes it through the input buffers, comparators, and latches, and stores it in the prememory. The Record control logic (including the combinational trigger logic, arm logic, and trigger delay counter) controls the storage of the data from the prememory into the main memory in response to the specified mode of operation.

The Display control logic is held reset by the Record control logic when the data is being recorded (written into the memory). When it is not held reset, the Display control logic will transfer the data from the memory to the display generator and will generate the necessary control signals to display the data.

The Digital Data Output logic can override the Display control logic (except when held reset by the Record control logic) and transfer the data from memory to the data output lines under control of the "Command" and "Request" inputs.

Figure 7.1B shows the physical locations of the various functions on the main board and the control board.

The 851-D uses three logic families: ECL 10K, Schottky TTL, and CMOS. To achieve the desired high-speed performance, ECL circuitry is used for all of the data processing and the Record mode control logic. Schottky TTL has adequate performance for the memory and is used because it is more cost-effective than ECL memory. CMOS is used for the control logic, where high speed is not needed, because of its low cost and simple interface with the ECL circuits. The memory subsystem operates off of +5 V and all the rest of the logic operates off of -5.2 V. Positive logic convention is used; i.e., the more positive level is a logic "1" and the more negative level is a logic "0". Level translators are used for signals going to and from the memory and for signals from ECL to CMOS. Translators are not necessary for signals from CMOS to ECL. Figure 7.1C shows the types of level translators used.

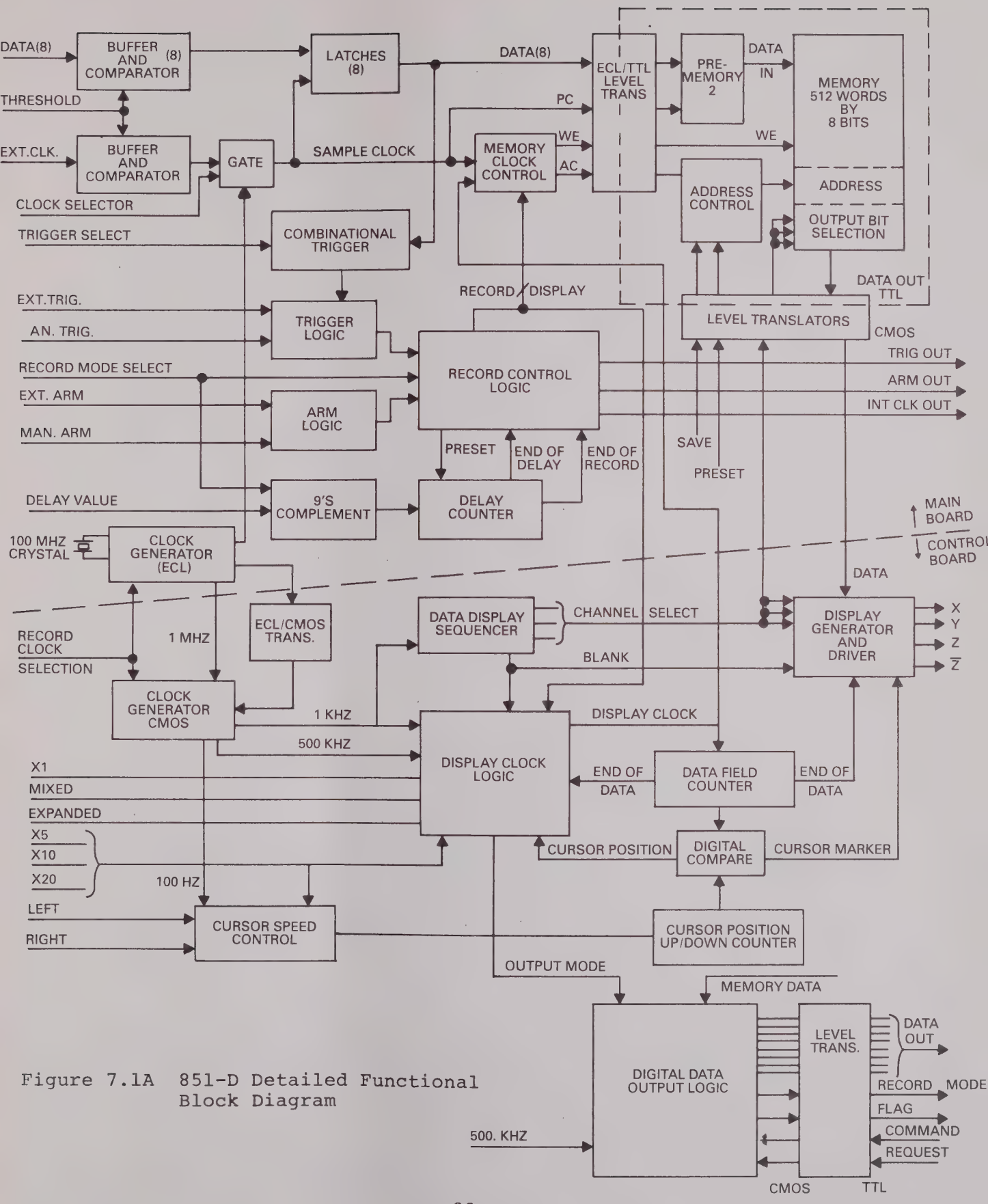


Figure 7.1A 851-D Detailed Functional Block Diagram

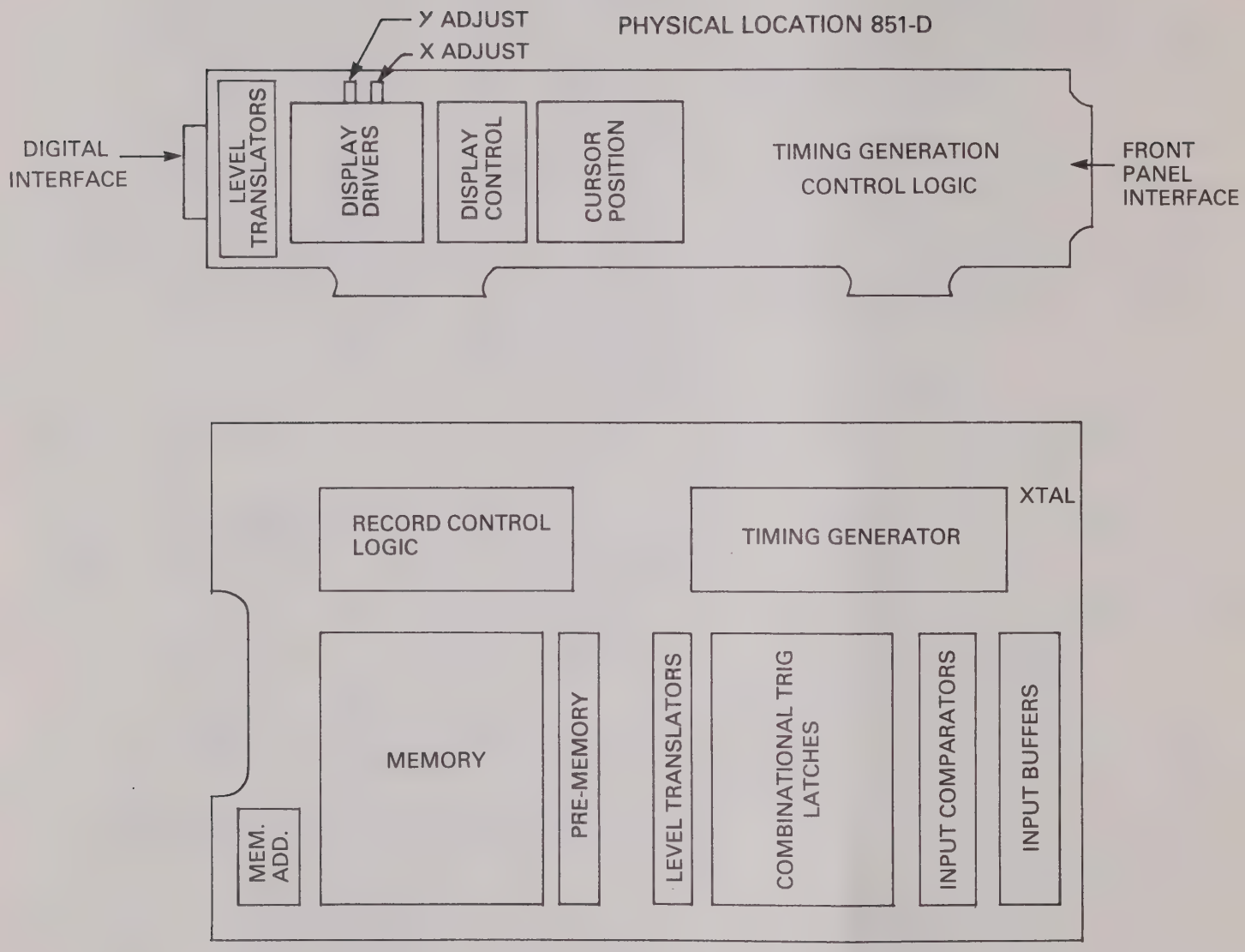


Figure 7.1B Physical Locations on the Main Board and the Control Board

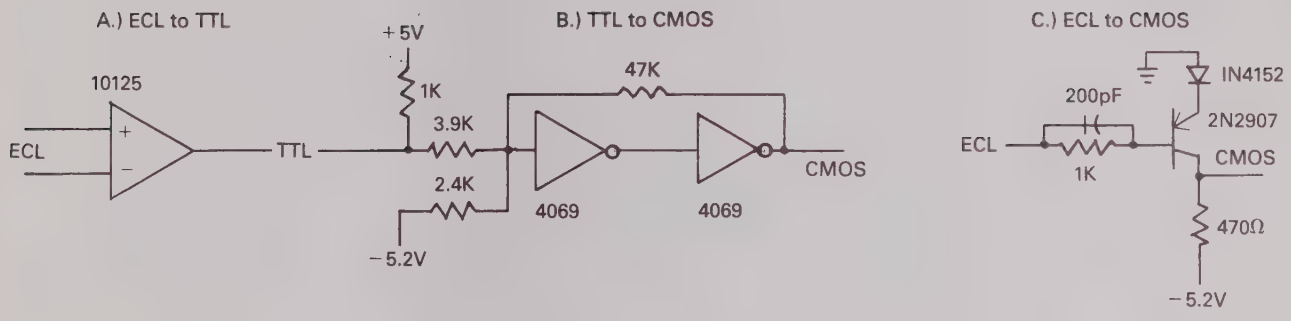


Figure 7.1C Level Translators

7.2 Detailed Description

7.21 Front Panel

The front panel assembly consists of two printed circuit boards and the front panel. The boards are called the "front panel board" and the "digitswitch board." The front panel board provides the mounting and interconnection of all of the control switches except the trigger delay digitswitch. The interconnection of the front panel switches to the control board is done by a PC edge-card connector between them. The combinational trigger selector switches are connected directly to the main board by a 16-conductor flat cable that plugs into a socket on the main board.

The digitswitch board contains the digitswitch and the threshold voltage circuitry. The threshold selector switches are connected to the digitswitch board by a 30-conductor flat cable that is soldered to both boards. The threshold levels are returned to the front panel board by that same flat cable and then passed to the control board by the edge-card connector and, in turn, passed to the main board by J2 of the control board. The delay selecting digitswitch is connected from the digitswitch board to the main board by a 16-conductor flat cable that is plugged into a socket mounted on the main board. Test points are provided on the digitswitch board to monitor the supply voltages and the threshold voltages.

The two boards are connected to each other by the 30-conductor flat cable, and normal servicing is done by using that cable like a hinge and opening the boards. If the boards are to be operated in this position, a ground connection MUST be provided between the two boards.

The threshold voltage circuit is shown in the schematic in Section IX. Resistors R10 and R11 drop the voltages supplied to R1, 2, and 3 to about +2.5 V and -2.5 V. The thresholds for these positions (TTL, ECL, MST) can be set anywhere between these voltages. This provides thresholds for use with X1 probes. The thresholds for use with X10 probes are set by R4, 5, 6, 7, 8, 9. To provide greater resolution for these adjustments the voltages supplied to the resistors are reduced to +0.5 V and -0.5 V by the circuits of U1, R12, R13, R14, and R15. The front panel variable threshold uses a circuit similar to that of R1.

7.3 Control Board

Refer to the Control Board Schematic in Section IX for the control board description. With the exception of the ECL to TTL level translators, the control board is all CMOS circuits

and the logic levels encountered will be 0 V for logical one and -5.2 V for logical zero.

The timing generation is divided into two parts. The main board contains the high-speed timing and provides the control board with a 1-MHz clock. The control board then divides this clock down to provide 100-kHz, 10-kHz, 1-kHz, and 100-Hz signals. The control board receives the time base selector switch signals from the front panel board, and the logic generates control signals that go to the main board to select the desired clock signal for the data sampling clock. The display control logic uses the 500-kHz clock as the basic data output clock and the 1-kHz clock for the display horizontal sweep rate. The horizontal sweep is generated as a 1-msec ramp of 1-V amplitude with a 1-msec blanking time between sweeps. The amplitude of the horizontal sweep is adjusted by R26 from 0.7 to 2.5 V. The 1-msec blanking time allows for retrace time in the display when an oscilloscope is used in the triggered sweep mode. The display blanking signals Z and $\overline{Z}$ are generated by the counter A5 as a square wave with 1 msec on time and 1 msec off time. The counter A5 controls the display sequence by simply counting the 1-kHz clock.

The display sequence is:

A5 0123	Count	Channel Selected	Display
0000	0	8	Blanked
1000	1	8	Data displayed with 0 V offset (normally at the bottom of the display)
0100	2	7	Blanked
1100	3	7	Data displayed with 0.1 V offset
0010	4	6	Blanked
1010	5	6	Data displayed with 0.2 V offset
0110	6	5	Blanked
1110	7	5	Data displayed with 0.3 V offset
0001	8	4	Blanked
1001	9	4	Data displayed with 0.4 V offset
0101	10	3	Blanked
1101	11	3	Data displayed with 0.5 V offset

A5 0123	Count	Channel Selected	Display
0011	12	2	Blanked
1011	13	2	Data displayed with 0.6 V offset
0111	14	1	Blanked
1111	15	1	Data displayed with 0.7 V offset
0000	0	8	Blanked
1000	1	8	Data displayed with 0 V offset
0100	2	7	Blanked
⋮	⋮	⋮	⋮

The display driver for the vertical axis (Y axis) consists of an op amp B3 with an output buffer transistor Q1 to provide increased output drive. Resistor R40 is provided to damp potential ringing on the output cable. The output may be modified to drive a 50-Ω input by changing R40 to a lower value (typically 10 Ω). The amplitude of the vertical output may be adjusted by R25 from 0.75 to 1.25 V full scale. Capacitor C9 provides some additional frequency roll off to shape the vertical edges of the data display. The display vertical position is determined by the sum of the currents introduced to the summing junction by the logic. Because of the simple resistive output characteristics of the CMOS gates, the hex inverter B6 is used to switch the input resistor either to ground (for no current) or to -5.2 V.

7.31 Display Mode Control

The display mode control logic is held at reset whenever the 851-D is recording. The record mode control logic on the main board supplies the signal "Record Mode C" to the control board for this purpose. The display mode logic becomes active whenever this signal goes low. The flip-flop of C9 provides a synchronized start up of the display mode with the 1-kHz clock. On the first 1-kHz clock after Record goes low, the output of C9 pin 15 goes high, and the signal SAVE B is sent to the main board to save the memory address at which the record mode ended. Also, a pulse is generated by C18 and R41 to initiate the memory address preset cycle. On the second 1-kHz clock, the output C9 pin 1 goes high, and the counter A5 is allowed to begin normal display sequencing. The display sequence will always start at count zero because the counter is held reset during record mode.

A "blank" cycle always precedes a display cycle. At the beginning of every blank cycle, a pulse is generated by C10 and R35 that will preset the flip-flop A14B (and also flip-flop J1 on the main board) to start the memory address preset cycle. The signal PRESET ADDRESS will remain high for five clock cycles of the 500-kHz clock and will allow the memory to be clocked five times to preset properly the memory address. Figure 7.2 shows timing diagrams for the memory clock operation in the display modes X1, MIXED, EXPAND.

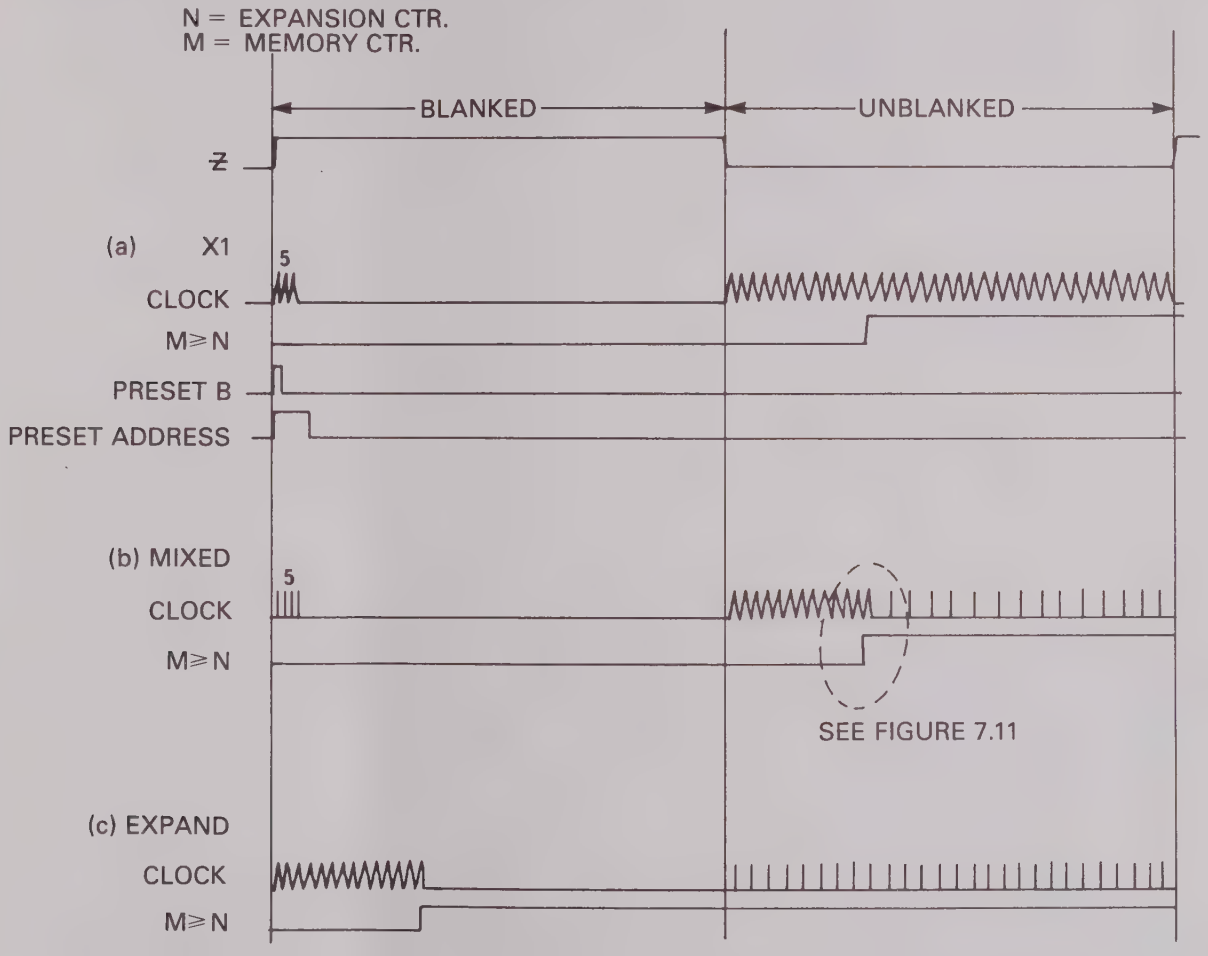


Figure 7.2 Display Memory Clock Generation

In X1 mode, the memory is clocked five times at the beginning of the blanking cycle, and then no more clocks are generated until the display is unblanked. At this time, the memory is clocked at the 500-kHz rate for the entire display time. This provides exactly 500 clock pulses during the display in X1 mode. The memory address is then preset again at the beginning of the next blank time.

In MIXED mode, the memory address is preset as in X1 mode, and then no more clock pulses are generated until the display is unblanked, at which time the memory is clocked at the 500-kHz rate until the memory position counter (A10, A11, and A12) is equal to the cursor position counter (C10, C11, and C12). At that time the clock rate is changed to either 100 kHz, 50 kHz, or 25 kHz depending on which expand is selected on the front panel (X5, X10, or X20). The circuitry for generating these clock rates is shown on sheet 1 of schematic 0852-0011 and consists of A20, B20, B21, B22, and parts of B19, C19, and A15. The counter formed by A20 and B20 is programmed by the select logic to divide the 500-kHz clock by either 5, 10, or 20 and then enable the 500-kHz clock for a single clock. Refer to Figure 7.3.

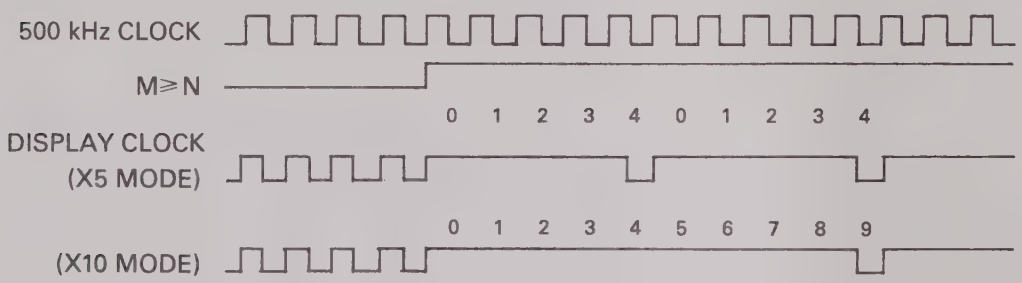


Figure 7.3 Memory Clock Details in MIXED Mode

In EXPAND mode, the memory address is preset at the beginning of the blank cycle, and the memory is then clocked at the 500-kHz rate until the memory position counter equals the cursor position counter, at which time the clock is disabled until the display is unblanked. Then, when the display is unblanked, the memory is clocked at the rate determined by the selected expand (X5, X10, or X20) as described above.

7.32 Cursor Position

The cursor position counter is shown on the schematic in Section IX and consists of A17, A16, A18, A19, B13, B15, B16, B24, C10, C11, C12, C13, and C14. The cursor position counter is an up/down counter and is controlled by the horizontal position switch on the front panel. When the switch is pushed to the right, the counter will be counted up, and when the switch is pushed to the left, the counter will be counted down. A contact bounce elimination circuit is used to condition these inputs to ensure proper operation. The flip-flops B24A and B24B sample the switch contacts at a 100-Hz rate and ensure the elimination of any bounces in between samples. Counters A16 and A17 are held preset to 4 counts less than top count (TC) until the switch is activated.

When the switch is activated, in either direction, the counter is allowed to count. When the count reaches TC, a single pulse will be allowed to count the cursor position up or down. The counters will then continue to count until A16 reaches count 2, at which time A16 will be stopped and the cursor position counter will be continuously clocked, at the selected rate, until the switch is no longer activated. Refer to Figure 7.4. If the switch bounces or is released, the counter will be preset again and the process must be started over. This gives a cursor "hesitation," allowing the operator to reliably achieve a single count. The rate at which the cursor position is clocked is determined by the circuit in such a way as to give a constant rate of motion of data on the display (2 cm/sec on an 8x10 display) in expand mode regardless of the selected expand.

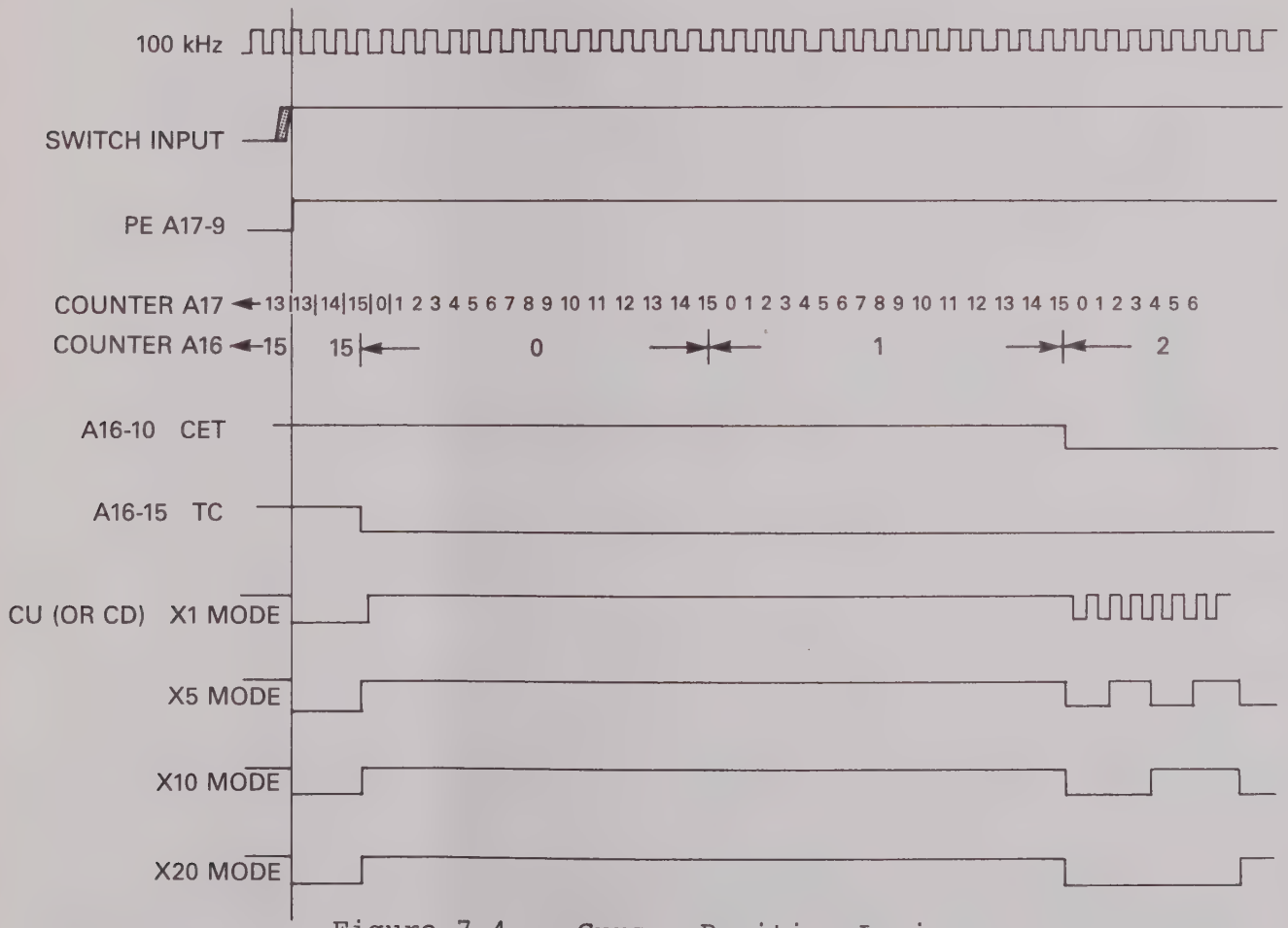


Figure 7.4 Cursor Position Logic

In X1 mode, the rate is 100 Hz, in X5 mode the rate is 25 Hz, in X10 mode the rate is 12.5 Hz, and in X20 the rate is 6.25 Hz. These rates are not exactly the same as the X5, 10, 20 expand ratios. They are, instead, X4, 8, 16 because it is much simpler to use a binary counter, and the slight change in apparent data motion speed is not noticeable.

A power-on reset circuit C12 and R36 resets the cursor position to zero (off the left side of the display) when power is turned on. When the cursor position is at zero, any attempt to count it down will cause a signal on the reset line and will prevent it from going past zero. Similarly, when the counter is at count 511 it will not be allowed to count up.

By allowing the memory position counter to count the memory preset clocks at the beginning of each blank cycle, the cursor appears to be positioned 4 counts to the left of the beginning of the data. This allows the cursor to "disappear" by positioning it off the left side of the display. It also means that it will not be seen on the screen until the fourth pulse.

7.33 Digital Data Interface

The digital data interface uses all TTL signals. The control logic is on sheet 3 of schematic 0852-0011 and the data output logic is on sheet 4. Because the memory is organized to read out a single data bit at a time, it is necessary to sequentially read out the eight data bits and shift them into a shift register C2 to provide a parallel output. The counter A5 is used to control this sequential operation. Refer to the timing diagram in Figure 7.5. The DUMP COMMAND input is active low. When it is active, it will allow the flip-flops of B9 to initiate the dump operation. The first clock pulse of the 500-kHz clock after Command goes low will set B9 pin 14 low, and this will enable the output shift register and the control logic for A5. This will generate a memory address preset signal.

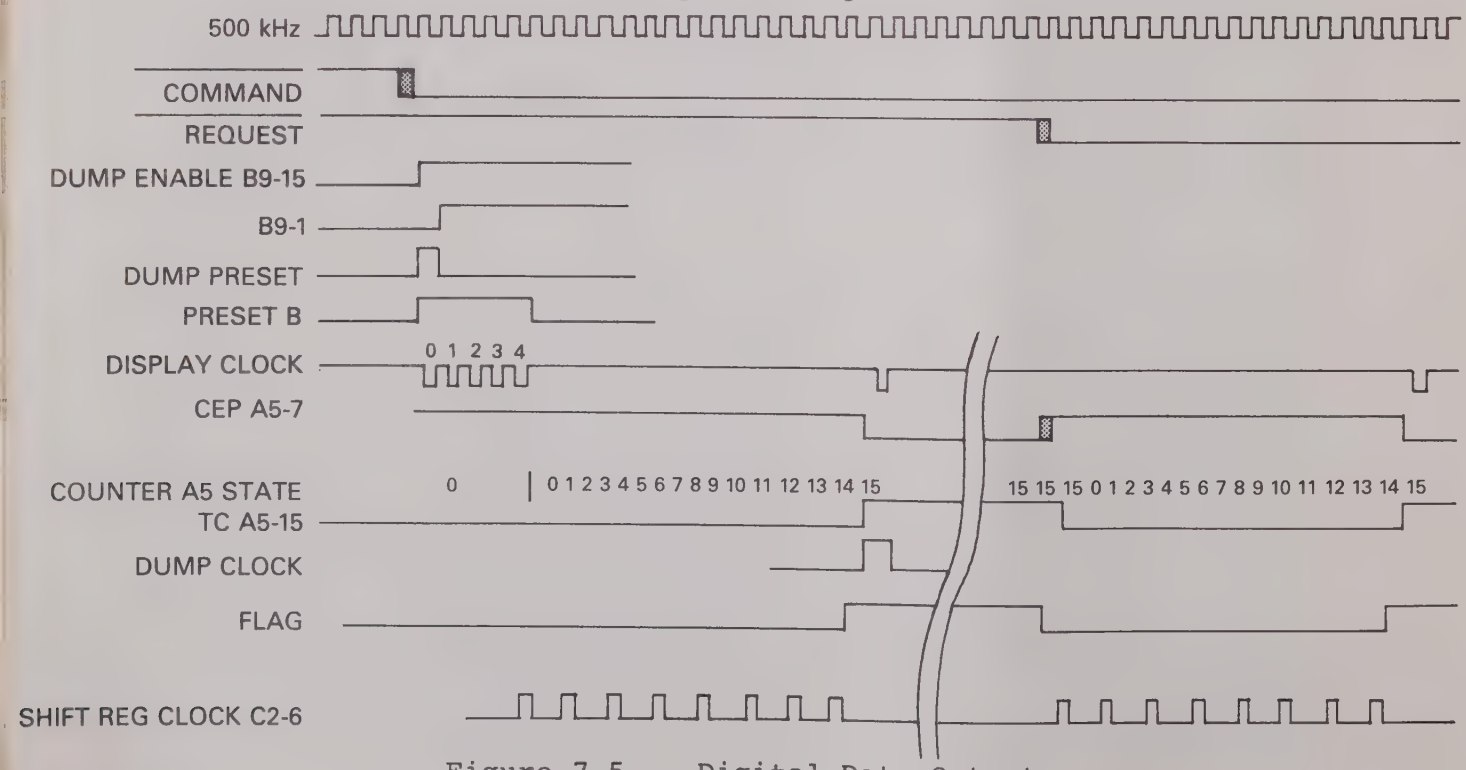


Figure 7.5 Digital Data Output

The memory address preset will generate five clocks to the memory in the same manner as during normal display operation. The second clock of the 500-kHz clock will cause B9 pin 1 to go high and pin 2 to go low, will remove the memory preset signal, will enable the 500-kHz clock to A5, and will disable the the 1-kHz clock from A5.

The preset address signal on A14 pin 15 will hold A5 reset until the memory preset cycle is complete, at which time the counter will count up to TC (count 15). Figure 7.5 shows how the data is clocked into the shift register. When the counter reaches TC, the counter will be disabled until the REQUEST line goes low. The TC output is translated to TTL level and put out on the interface as the FLAG signal.

The output data may be clocked with the leading edge of the FLAG signal. The output data will be stable at least 500 nsec before the FLAG signal goes high and will remain stable for at least 500 nsec after the FLAG signal goes low. The input control lines COMMAND and REQUEST are translated from TTL to CMOS by Schmidt Trigger level translators A4 as described in Section 7.1.

7.34 Display Synchronization

A display sync input is provided in the digital interface connector (pin 15). To sync the display of two 851-D instruments, all that is necessary is to connect the Z output of the "master" unit to the display sync input of the "slave" unit. The positive going transition of the display sync input will generate a pulse, and if the 851-D is in display mode, this pulse will reset the counter chain of A21, A22, A23, and A24. This will cause the two instruments to run in sync.

7.4 Main Board

Refer to the main board schematic in Section IX.

7.41 Input Buffer

The input buffer circuits are the same for all eight data channels and the external clock input. Operation of data channel one will be described.

Resistors R101 and R102 and diodes CR101 and CR102 establish the input impedance at 1 MΩ and also provide protection against input voltages as great as 100 V for short duration, 50 V continuous. The main limitation on the input protection is the power dissipation in R102. Capacitor C102 provides frequency compensation for R102. Capacitor C101 allows adjustment so that all inputs have the same capacitance. Q101, R105, R106, and R113 make a zero offset FET source follower circuit. R113 allows fine adjustment of the offset voltage.

7.42 Comparator

Diodes CR103 and CR104 protect the inputs to the comparators and clamp the voltage to approximately ±3 V. The clamp voltages are generated by the op amps A25A and A25B and resistors R20, R21, R25, and R26. The nominal values of the clamp voltages are +2.6 and -2.5 V. Resistors R103 and R107 provide hysteresis. Because the outputs of the comparator are ECL signal levels (-1 and -2 V), the hysteresis circuit introduces an offset error of approximately 10 mV, and this must be corrected by the adjustment of the input buffer offset R113. The comparator provides complementary ECL outputs, and resistors L20-14 and L20-13 are the pull-down resistors.

7.43 Latch/Sample

The Latch/Sample circuit is formed by flip-flops L18A and L18B as well as gates L21, and is controlled by the signal SAMPLE MODE ENABLE from the front panel switch. When the signal is high, the circuit is in sample mode, and when it is low, the circuit is in latch mode. In sample mode, the gates L21 are disabled and their outputs are low. This allows the first flip-flop L18A to operate in the clocked mode, and the data present at the input at the time of the positive clock transition will be clocked into the flip-flop. The second flip-flop simply passes the data on one clock pulse later.

In the latch mode, the gates L21 are enabled, and the first flip-flop acts as a latch that changes its output whenever it detects that the input data is different than it was at the last clock transition (as stored in the second flip-flop). Figure 7.6 shows the operation for several different inputs.

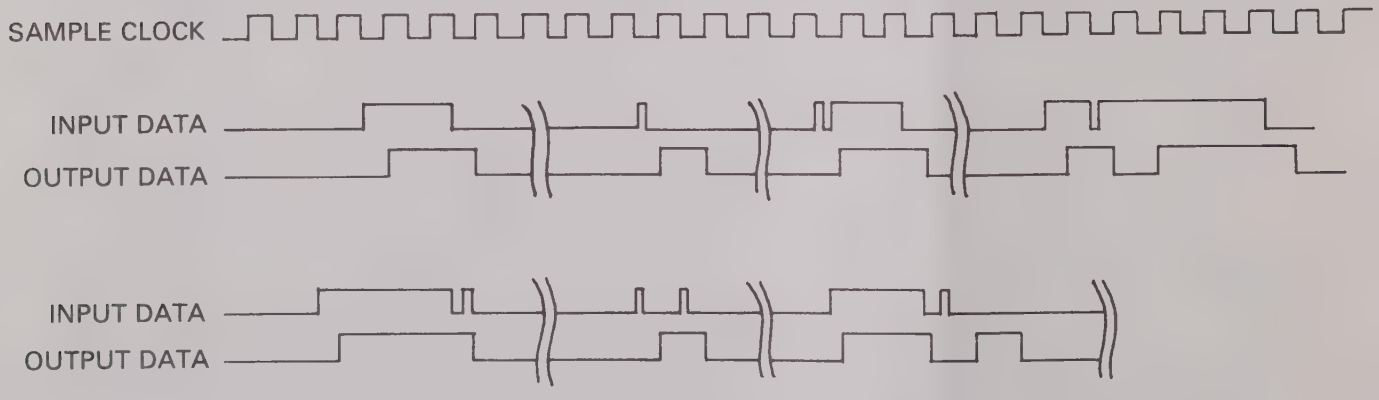


Figure 7.6 Latch Mode Operation

7.44 Combinational Trigger

The Combinational Trigger circuit is L16, L17 (and the same gates on the other seven channels), A8, A7. Gate L17 will

generate a low output if the data on L18 output is high and the selector switch is in the "1" position or if the data is low and the switch is in the "0" position. The combinational trigger gates L17, K17, J17, H17, F17, E17, D17, and C17 are all connected together in a "wired-AND" such that the selected trigger conditions of all eight channels must be true for the signal TRIGGER NODE to go low (true). The flip-flops A8A and A8B provide two functions. The first flip-flop synchronizes the data to the sample clock and eliminates the propagation delay effects of the "Trigger Node." The second flip-flop allows the detection of Trigger Node transitions by the gates A7.

Either positive or negative transitions are selected by the front panel switch "INT T" or "INT F."

7.45 Timing Generation

The internal timing generator is shown in Section IX and consists of the crystal Y1, R22, R23, L1, C24, C41, and the ICs A24, A23, A22, as well as the level translator Q5. The resonant circuit formed by L1, C24, and C41 is to ensure that the crystal does not operate at one of its lower harmonics. The crystal operates at the sixth overtone. Resistors R22 and R23 provide bias for the gate A24. Resistor R24 is simply a pull-down. The complementary output (pin 9) of A24 is used to avoid loading effects on the oscillator. The counters A22 and A23 simply divide the oscillator by 10 and 100 to provide the 10-MHz and 1-MHz clock rates.

The gates of A20 are used to select between 100 MHz, 10 MHz, 1 MHz, and 100 kHz, and gate A24 selects the low-speed clock rates from the control board. The flip-flops A18 and A19 generate rates of one-half and one-fifth of the selected clock. Then the gates of A16 select the 1, 2, or 5 division as specified by the control board. Gates A15 and A24 allow the selection of INT, EXT∫, or EXT⌇. Gate B19 is used to drive the coax cables to distribute the clock to the input latches.

7.46 EXT ARM/EXT TRIG

The inputs for EXT ARM and EXT TRIG are especially configured to allow either TTL or ECL inputs. Because the ECL and TTL input circuits are wire-or'ed, only one of them may be active at a time. (The other one may be left disconnected.)

The EXT TRIG input stage operates in the following manner. TTL input is applied to pin 11 of the digital I/O connector on the rear panel. The signal is passed from the control board to the main board by J1-E to resistor R43 and the base of Q3. R43 is a pull-up resistor to +5 V and will maintain the input inactive (high) when no input is connected. The resistors R44 and R45 establish a bias point of +2.5 V on the emitter of Q3 and

set the input threshold level. As long as the input is higher than +2.5 V, Q3 will be off and will not affect any signal that may be input on the ECL input. When the TTL input goes low, then Q3 will conduct and its collector current will be set by R44 and R45 (typically 20 mA for an input low level of 0.8 V). This current will raise the voltage of the input pin 11 of C8 to about -1.0 V as a result of resistors R3 and R4, which form an equivalent termination of 50 Ω to -2.0 V. For ECL input signals, the termination of R3 and R4 will correctly terminate an ECL output driving a 50-Ω cable.

The EXT ARM input stage operates in the same way as the EXT TRIG input.

7.47 Memory

The memory subsystem is multiplexed to achieve the required writing rate of 50 MHz. The result of this is that the memory ICs only have to operate at 25 MHz because the data is alternated between two memory ICs.

The memory multiplexer operates as follows. In record mode, the sample rate clock is applied to both flip-flops of B16, and these flip-flops are connected to change state on every positive transition of the sample clock. The data holding registers (referred to as prememory) are clocked by the signals PC1 and PC2 from the level translator B15. Because PC1 and PC2 are complementary signals, the data registers will be clocked alternately by the positive edges of the sample clock.

A typical operation would be: At the positive edge of the sample clock, the flip-flops are set such that PC1 goes true and PC2 goes false. The data will be strobed into the prememory 1 by PC1 and the previous data, already strobed into prememory 2, will be written into the memory by the signal WE2. On the next positive edge of the sample clock, PC1 will go false and PC2 will go true. The new data will be strobed into prememory 2, and the data already stored in prememory 1 will be written into the memory by WE1. Thus, on each clock, the new data is stored in the prememory, and the previous data is written into the memory.

The memory address operates in a similar manner. On the same clock that sets PC1 true, AC1 is also set true, and AC2 set false. When AC1 goes true, the address is stored in address-holding register 1 and the address counter is incremented. On the next clock, AC2 goes true and stores the new address in address register 2. The newt clock will store that address in register 1 and increment the address again. Thus, the data and address registers for memory 1 are both clocked together and the write enable pulse for memory 1 is brought active on the next clock pulse. The level translators for write enable and chip select are gated on and off by a resistor network R17, R18, R41,

and R42. When RECORD MODE is low, the level on pin 11 of B15 is -1.3 V and the translator functions normally. When the level is high, pin 11 is at -0.66 V, and the outputs are held high. During record mode the chip selects are both held low.

In display mode, i.e., when not recording, the write enable level translator is disabled and forced to high outputs. The level translator for the chip select is enabled to allow alternately selecting the memories for readout. The memory address clock is switched from the sample clock to the "display clock" by simply disabling gates B18, forcing flip-flop C10 to follow the sample clock during record mode. The display clock is generated by the control board and flip-flop C10 to provide the multiplex action. The chip select signals CS1 and CS2 are active low and operate in much the same way as the write enable signals during record mode. For example, on the positive edge of the display clock, AC1 will go true and AC2 will go false, and the memory address will be incremented. On the newt positive edge, AC2 will go true and CS1 will go false, the address will be clocked into memory 2, and the data will be read from memory 1 until the next clock. At the next clock, the address will be clocked into memory 1, the address will be incremented, and the data will be read out from memory 2. The data is alternately read from memory 1 and 2.

To be able to restart the memory at the correct memory address, the "end of record" address must be saved. Both the memory address counter and the memory multiplexer phase are necessary. The signal RECORD MODE is connected to B16 pin 6 so that when record mode ends the flip-flop will be disabled. Thus, the multiplex phase will be maintained in this flip-flop until record mode starts again, and, because the address counter is clocked by this flip-flop, the address counter will be stopped. The memory address must then be saved in registers L2 and K2 before the display clock is initiated. The signal SAVE A is generated by the control board and strobes the memory address at the end of record into the register. To restart the memory, it is necessary only to transfer the memory address from the registers to the counter and to preset flip-flop C10 to the state of flip-flop B16. Because the counter has a synchronous preset, it is necessary for flip-flop J1 to hold the preset enable on the counter until it is preset by clock AC1.

7.48 Record Control Logic

The record mode control logic is shown on the schematic in Section IX and has three major control signals: ARMED, ENABLE DELAY COUNTER, and RECORD MODE.

The control signal ARMED is generated by A4 pin 15. The ARMED signal may be activated at any time by the manual arm switch or by the TTL external arm input, which is the ECL external

arm input. It may be activated by the auto arm signal if it is not already armed and the delay counter is not enabled. The circuit is latched in the ARMED condition until a trigger signal is received and the delay counter is enabled, at which time the ARMED latch is reset. The output of A3 pin 7 is connected to B5 pin 13 and prevents the acceptance of a trigger signal as long as the manual arm or the external arm signals are active.

The ENABLE DELAY COUNTER signal is activated (set true) by the trigger signal applied to B5 pin 10. It is reset by the "end of record" signal applied to B5 pin 11, and is clocked by the positive edges of the sample clock. When the delay counter is enabled, B5 pin 15 goes true and causes the ARMED latch to be reset, the auto-arm signal to be disabled, and the delay counter to be changed from preset mode to count-up mode.

At the same time, B5 pin 14 goes false and enables gate A5 to generate the start record mode signal when in the delay trigger mode. The "end of record" signal is generated by gates B8 and C8 depending on the mode selected (pretrigger or delayed trigger). For pretrigger mode, the end of record signal is decoded as count 508, and for delayed-trigger mode the count 511 is decoded.

The delayed-trigger counter uses flip-flop C10 to generate the "ripple" clock for counters B10, B11, B12 because the carry out signal has too much propagation delay for operation at 50 MHz. However, because the preset is synchronous (requires a clock), during preset mode it is necessary to gate the flip-flop inactive (by holding it preset) and to introduce the sample clock to drive these three counters.

The RECORD MODE signal directly controls memory for recording and allows the control board to generate the display control signals when not recording. RECORD MODE is set true in pretrigger mode whenever the signal ARMED is true. In delayed trigger mode when the delay counter is enabled and reaches TC, the same thing occurs.

The delay counter in delay mode will be preset to a value that will require the selected number of clocks after trigger to reach TC. This preset number is generated by taking the "tens complement" of the front panel digitswitch. Circuits A9, A10, A11, and A12 perform this function when delay trigger mode is selected. When pretrigger mode is selected, they present the digitswitch information to the counters unchanged.

7.5 Power Supply

The power supply is a series pass type and has foldback current limiting and overvoltage crowbar protection. The circuit will maintain regulation with only a 0.6 V drop from input to

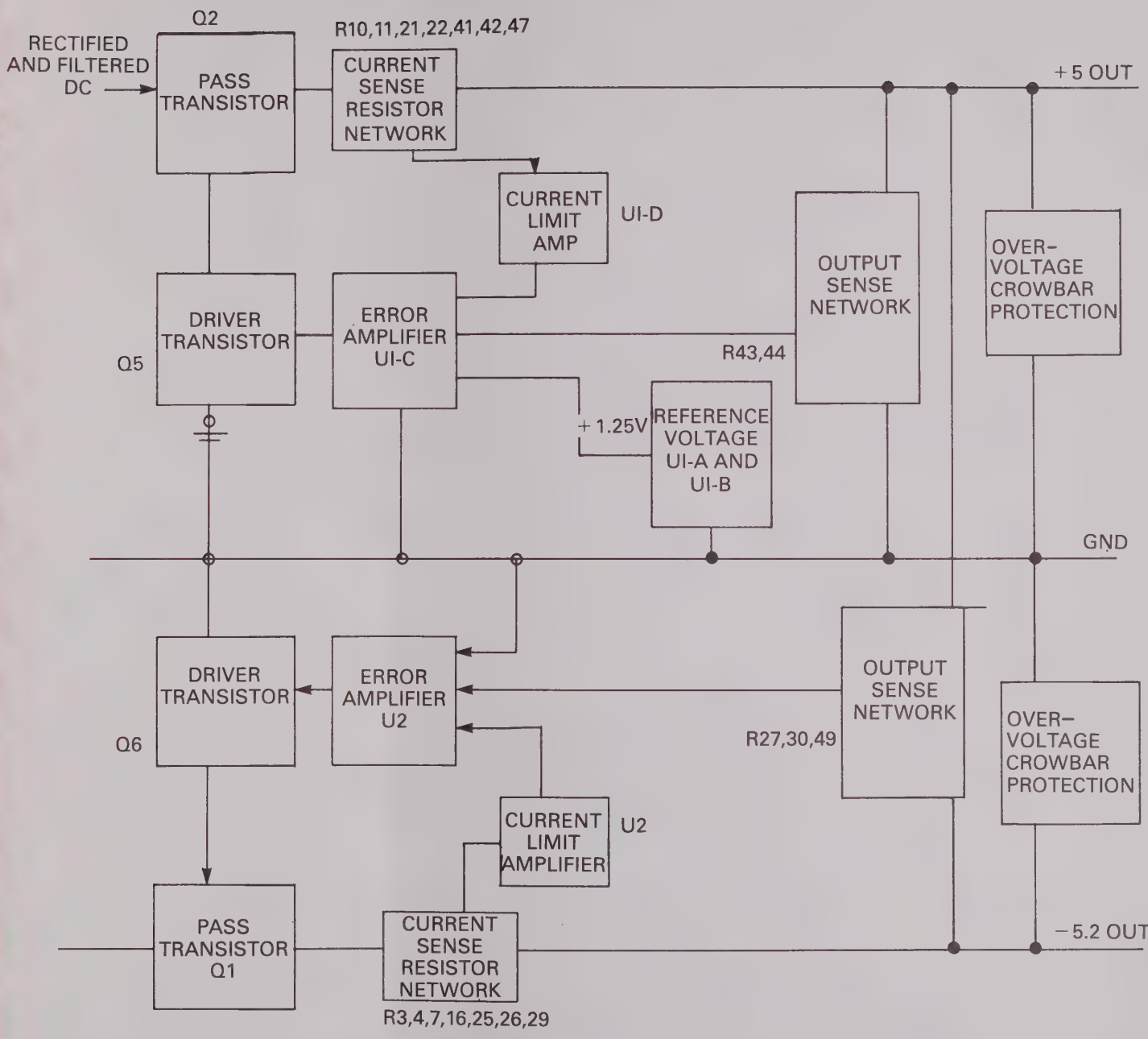


Figure 7.7 Power Supply Block Diagram

output, thus enabling the supply to achieve good efficiency. Figure 7.7 is a simple block diagram of the regulator circuit. The negative regulator is very similar to the positive regulator and is connected so that the negative output tracks the positive output. There are two adjustments for the output voltages. The positive output is adjusted by potentiometer R37, and the ratio of the negative output to the positive output is adjusted by potentiometer R49.

Figure 7.8 is a simplified schematic of the positive regulator circuit. The configuration of the pass transistor Q2 and the driver transistor Q5 is especially chosen to allow operation with the minimum voltage drop from input to output. The resistor R18 is necessary to limit the base current to Q2 during turn on and in case of very low input voltage. A Darlington transistor is used for Q5 to provide sufficient current gain to drive the pass transistor into saturation at a 5-A output. The pass transistors are mounted to a heat sink directly in front of the fan and are electrically insulated from the heat sink. The driver transistors are mounted on a small heat sink on the printed circuit board and are also insulated.

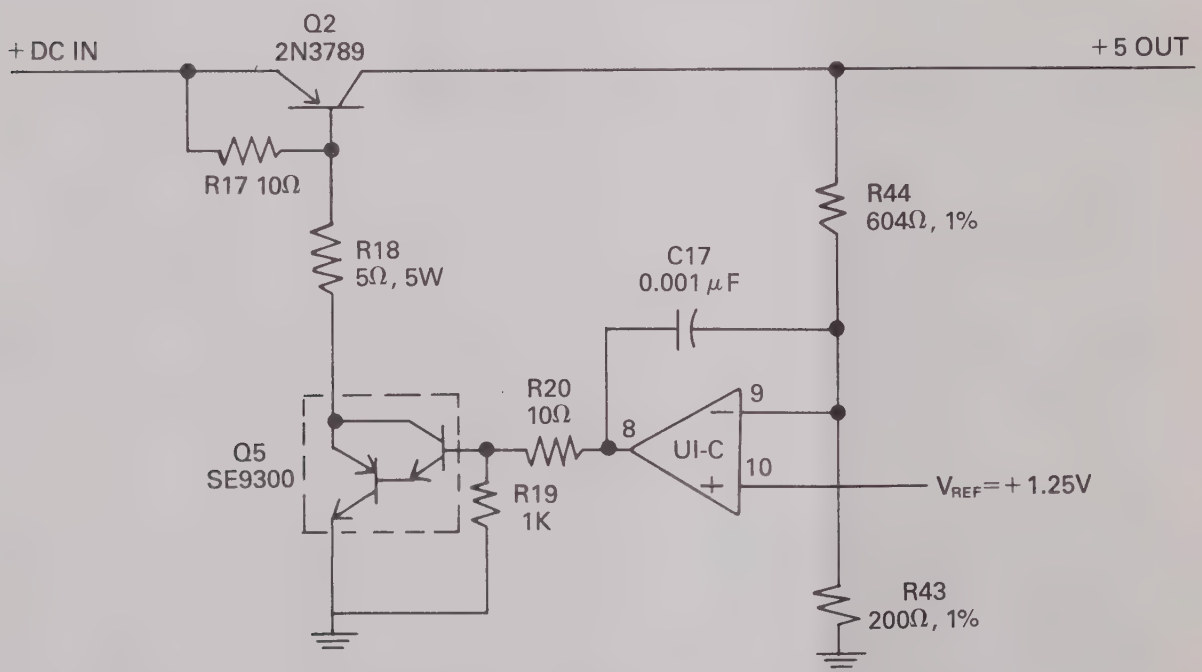


Figure 7.8 Simplified Schematic - Positive Regulator

The reference voltage circuit consists of two op amps and a monolithic dual diode. Refer to Figure 7.9. The dual diode CR9 provides a temperature stable reference in the following way.

The reference voltage circuit makes use of the temperature tracking of the two diodes and, by setting the current level in each diode properly, achieves a cancellation of the temperature coefficients of the two diodes.

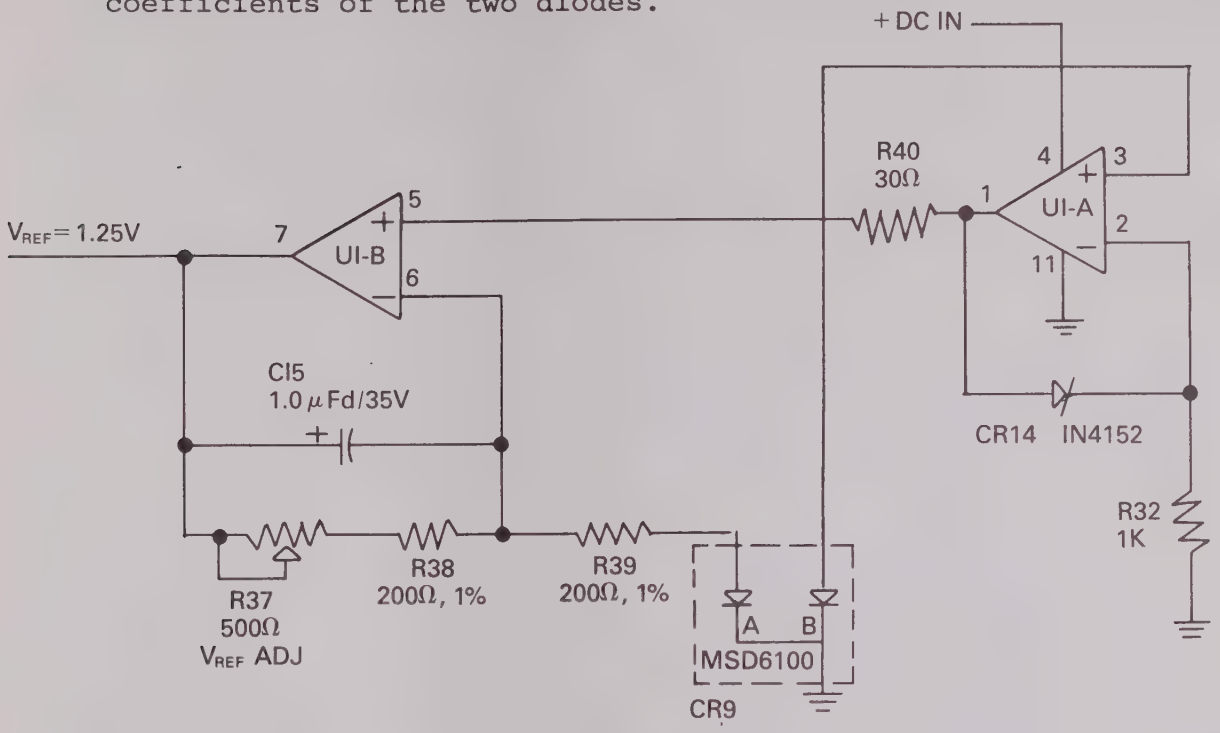


Figure 7.9 Schematic - Reference Voltage

To provide reference stability with respect to input voltage changes, a current source is formed by the op amp Ul-A and resistors R31, R32, and R40. This provides a constant 20 mA to diode "B." The reference voltage output as a function of input voltage is shown in Figure 7.10.

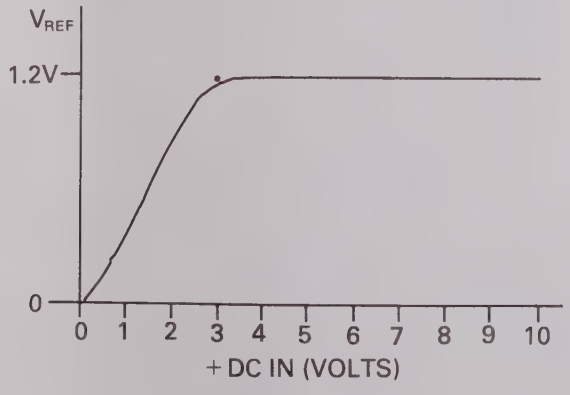


Figure 7.10 Reference Voltage Versus Input Voltage

In normal operation, the op amp U1-C compares the reference voltage to the feedback voltage (from R44 and R43) and controls the driver transistor Q5 in such a way as to maintain the output voltage at the desired value. If the output is low, the op amp U1-C will go more positive and cause Q5 to pull more current from the base of Q2, thus causing Q2 to provide more current to the output to raise the voltage. The resistor R9 provides current to the output to ensure startup.

The current limit circuit consists of op amp U1-D and resistors R10, R11, R21, R22, R41, R42, R47, R48, CR8, and CR13. The circuit acts as a differential comparator and when the voltage across R10 and R11 reaches the value determined by R21, the op amp will go positive and force the regulation to be controlled by the current limit circuit U1-D. The typical values of current limit are 9 A (450 mV) for +5 output and 6 A (300 mV) for -5.2 output. The diode CR13 and resistor R48 introduce additional current to the network to increase the current allowed at low-output voltages. This ensures startup. The resistor R50 in the negative regulator performs this same function.

The overvoltage crowbar circuit consists of Q4, CR6, R23, and C6 as shown in Figure 7.11. The SCR Q4 will be triggered when the output voltage reaches CR6 plus the gate trigger voltage of Q4 (about 1 V). This value is typically 7.2 V. This circuit is intended to protect the system in case of a failure of one of the pass transistors. If Q2 fails, the output voltage will rise until it reaches about 7.2 V, at which time the SCR will be fired and draw the output voltage down to about 0.9 V. Because the transistor Q2 has failed as a short circuit, the current limiting circuit will not function and the current drawn by Q4 will be determined by R10, R11, and the wiring resistance. This will normally be a large current (>10 A) and will cause the fuse to blow.

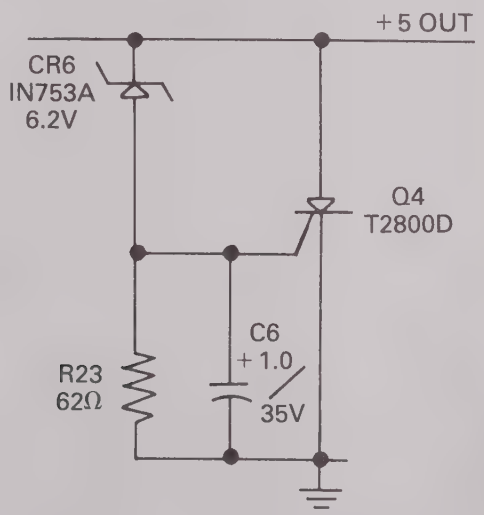


Figure 7.11 Overvoltage Crowbar Circuit

Provision for selecting the nominal line voltage of 100, 120, 220, or 240 V is provided in the AC power-plug unit on the rear panel. Also included in the AC power-plug unit is an RFI filter. The transformer is specified for operation from 50- to 400-Hz line frequency.

The power supply includes provision for remote sensing of the output voltages to eliminate the effects of voltage drop in the connecting lines. Resistors R46, R28, and R35 are included to establish the sense voltage in the event that the remote sense lines become disconnected. In this case the output voltages will increase by about 0.1 V.

SECTION VIII

MAINTENANCE PROCEDURES

8.1 Maintenance

This section covers maintenance and disassembly procedures for troubleshooting and repair of the Model 851-D. Repair is performed with the aid of a diagnostic procedure for the unit, a technical description, and a schematic diagram.

Waveform photographs have been included with the schematics to aid service personnel who wish to troubleshoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 255-9500 TWX 910 338-0226.

In summary, there are two methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Troubleshoot the problem to the component level with the aid of the troubleshooting procedure and schematics or with the aid of factory personnel.

8.2 Required Test Equipment

The following test equipment will be required to conduct the diagnostic procedure:

1. Two pulse generators capable of <1-nsec rise and fall times. A minimum pulsewidth of 2 nsec of output adjustable from -5 to +5 V into 50 Ω with single pulse capability.

2. An oscilloscope: 2 channel DC to 200-MHz input bandwidth. Horizontal resolution to 1 nsec.

3. Digital voltmeter: Range 0-20 V min, 4 1/2 digit resolution.

4. A frequency counter, range 1 to 100 MHz min.

If a display device is not normally used with the Model 851-D, an additional oscilloscope or CRT display will be required during the testing period. This latter oscilloscope need only have a 2-MHz input bandwidth.

8.3 Diagnostic and Troubleshooting Procedures

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

8.31 Equipment Setup

Connect a display device to the 851-D as per Figure 4.5. Turn on the 851-D and the display and allow them to warm up for a few minutes.

NOTE: Display may not be present at this time.

Set Front Panel controls as follows:

Trig Source - Int (T)
Record Mode - Delay Man
Delay - 0000
Threshold - TTL X1 Both CH 1-4 and CH 5-8
Int Clk - 0.02 μsec
Clock Source - Int
Display - X1

Press MAN ARM switch down. ARM ready light should come on. Press Man Trigger. Display should now look like Figure 8.1.

Arm light not illuminated.

Verify ECL Logic Low at IC A4 pin 14 (test point 31). Observe <-5.2 V DC at test point 63.

No display when triggered.

Verify ECL Logic High at IC B5 pin 3 (test point 30). Observe 1 msec square wave at IC A5 pin 14, and a binary count at pins 13, 12, 11 on IC A5. Verify waveforms as in photographs on the attached pages in Section IX (test points 1-4). Verify that waveforms at test points 7, 6, 8, and 9 are as in photographs.

Using a voltmeter check the threshold levels. Connect the voltmeter between ground and the CH 1-4 test point.

Level not to specification.

Adjust levels not correct by using calibration procedure in Section 6.5.

DIAGNOSTIC PROCEDURE

Threshold Control Position	Level and Test Jack
ECL (black)	-1.30 V ±0.025
TTL (black)	+1.40 V ±0.025
MST (black)	0.00 V ±0.025
ECL (red)	-0.130 V ±0.005
TTL (red)	+0.140 V ±0.005
MST (red)	0.00 V ±0.005
A (red)	+0.250 V ±0.005
B (red)	-0.250 V ±0.005
C (red)	+0.200 V ±0.005

NOTE: This applied to units of S/N 6038 and above.

Repeat above for CH 5-8 using CH 5-8 test point.

Set up front panel controls as follows:

Trig Source - Int (T)
Record Mode - Delay Auto
Threshold (both) - TTL X1
Int Clk - 0.02 µsec
Clock Source - Int
Display - X1
Combinational Trigger all to "X" except CH 1 to "1".

Set up pulse generator as follows:

Positive going pulse from 0 to +3 V. 1 µsec wide, 9 µsec apart. Input above pulse to channel 1. Output should be as shown in Figure 8.2. Change Combinational Trigger on CH 1 to "0". Output should be as shown in Figure 8.3. Continue this until all 8 channels' "1"s and "0"s have been checked, while leaving each channel checked into "0" position. Connect pulse to CH 1 input. Change Trig Source to INT (F). Set Combinational Trigger to "1" on channel 1. Output should be as shown in Figure 8.3.

TROUBLESHOOTING PROCEDURE

Waveform not as in Figure 8.2.

Observe waveform at IC A8 pin 7 (test point 10), as shown in photograph. Monitor test point 29 on IC B5 pin 7, 15 (see photograph). Observe waveform as on attached pages (test point 33). Monitor test point 35 for 1 msec waveform. Verify photograph at test point 30. Observe ≥+12 VDC at test point 61, and ≥-12VDC at test point 62.

Waveform not as in Figure 8.3.

Observe waveform at IC A8 pin 7 (test point 10), as shown in photograph.

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

8.32 Clock Interval

Connect a BNC "T" connector to the "Trig In" BNC on the rear panel. Connect a short (12" or less) BNC cable from the "Trig In" "T" to the "CLK OUT" BNC. Connect the vertical input of the scope to the other side of the "T" connector. This terminates the ECL output from "CLK OUT".

With the internal clock set at 0.02 µsec, the period of the output rate should also be 0.02 µsec as shown on an oscilloscope.

Waveform on scope face not 0.02 µsec period.

Monitor IC A18 pin 3 (test point 15), as in photograph. Monitor IC A16 pin 5 (test point 16) on attached page. Observe waveforms at test points 11, 12, 13, 14, 18-21 (each signal is divided by 10 from the previous waveform).

Check each setting of the Int Clk control in both µsec and msec.

NOTE: In each case the period of the waveform should equal the setting of the Int Clk.

Verify the following while changing the time base switch

Test point Lo (ECL) for INT Clk settings.

T. P. Clk Setting

22 - 10, 20
23 - 1, 2, 5
24 - 0.1, 0.2, 0.5
25 - 0.02, 0.05
26 - any "1" position
27 - any "5" position
28 - any "2" position

8.33 Record Mode Delay Insertion

Pre Trig Memory/Trig Delay

To check the delay, remove the top cover from the unit.

DIAGNOSTIC PROCEDURE

Connect the scope as follows:

CH 1 to main board IC B5 pin 15.
CH 2 to main board IC B5 pin 3.
Set Horiz. to 2 µsec/div.
Set scope to trigger on + slope of channel 1.

Set Front Panel controls as follows:

Record Mode - Delay Auto
Trig Delay - 0010
Int Clk - 1 µsec

Input a 1 µsec wide pulse 9 µsec apart. Output of scope should be as shown in Figure 8.4. Advance "units" digit of delay. Each digit should increase the width of the channel 2 pulse by 1 µsec; at "9" the pulse should be 11 µsec wide. Reset delay to 0000. Change Horiz. rate on scope to 10 µsec. Advance delay "tens" switch to 1. Pulse on channel 2 should increase slightly ≈1 µsec. Advance "tens" digit to "2". Pulse should now be 10.2 µsec wide,and increase 10 µsec for each digit; at "9" the pulse should be 80.2 µsec wide. Reset "tens" digit to 0. Set scope to 0.1 msec/div. Waveform should be as shown in Figure 8.5. Advance "hundreds" digit one step at a time. Width of positive pulse at left edge of channel 2 should increase 0.1 msec each step to a maximum of 0.9 msec. Reset hundreds digit to 0. Set scope to 1 msec/div. Advance "thousands" digit one step at a time. Width of positive pulse at left edge of channel 2 should increase 1 msec each step to a maximum of 9 msec. Reset "thousands" digit to 0. Remove scope probes from IC B5.

TROUBLESHOOTING PROCEDURE

Waveform not as in Figure 8.4.

Verify ECL Lo level at test point 32 (IC C8 pin 12). Verify CMOS logic high level at test point 53 (IC A9 pin 5). With all digit switches set 0000, verify test points 54-57 (ECL Hi, Lo, Lo, Hi respectively). Change delay to 0001, and verify that test points 54-57 are the 9's complement. Continue this procedure for all numbers (0-9) in ones and tens location.

Waveform not as in Figure 8.5.

Repeat above procedure with appropriate device and switch.

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

8.34 Pretrig Mode

Set Front Panel controls as follows:

Trig Source - Int (T)
Record Mode - Pretrig
Delay - 0250
Int Clk - 0.02 µsec
Combinational Trig - 1XXXXXXX.

Set pulse generator output to 3 V. 1 µsec wide pulse with repetition rate of 10 msec. With this pulse connected to the channel 1 input, manually arm the 851-D.

Display should go away as long as the ARM switch is held down. When it is released, the output should be as shown in Figure 8.6. Changing the delay to a lower number should cause the pulse to move to the left on the display. Increasing the delay should cause the pulse to move to the right.

NOTE: When the delay is changed, the new position must be reinstated in memory by use of ARM switch.

Waveform not as in Figure 8.6.

Verify ECL High Level at test point 32 (IC C8 pin 12). Observe test point 34 (see photograph). Verify "TTL" 25 MHz waveform at test points 40, 41. Monitor test points 64, 65 for "TTL" Logic High. Observe input signal (1 µsec pulse width at "TTL" level) has some jitter at test point 66. Observe gated waveform at test points 50, 51, and with scope synchronized (+) on test point 50. Monitor test points 42-49 (binary progression). Observe attached photograph for proper waveform at test point 37.

8.35 Delayed Manual

Set Front Panel controls as follows:

Record Mode - Delay Man
Delay - 0000

Input the 1 µsec pulse 9 µsec apart to channel 1. Manually ARM unit; output should be as shown in Figure 8.7. Advance "tens" digit of delay and manually arm unit.

Waveform not as in Figure 8.7.

Verify ECL Lo level at test point 32 (IC C8 pin 12). Verify ECL High Level at

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
Pulse on left should disappear off to the left and the pulse on the right should move to the left. Place Record Mode to Delay Auto. 851-D should continuously arm, trigger, record, and display data. Verify this by advancing "tens" digit on delay. Pulses should move without requiring MAN ARM. Return digit switch to 0000.	test point 53. Verify test point 67 has a CMOS Logic High Level.
	No rearming.
	Observe test point 33 (see photograph in Section IX).
8.36 Display	
Change pulse generator to a 0.1 µsec wide pulse. Adjust period until 20 pulses are on the display. Change Display switch to expand.	
Horiz. to X5 - 4 pulses should be on the display.	Horizontal expansion not correct.
Change Horiz. to X10 - 2 pulse should be on the display.	Verify test point 34 changes repetition rate within gated window as expansion factor changes (X5, X10, X20). Verify at IC B17 pin 11 (test point 52) a clock rate while cursor switch is depressed.
Change Horiz. to X20 - 1 pulse should be on the display.	
Change Display to Mixed. Change Horiz. to X5. Move cursor switch to the right momentarily four times. Display should be as shown in Figure 8.8 (cursor should be at left edge of screen). Move and hold cursor switch to the right. Mixed display as shown in Figure 8.9 should occur. Check to make sure that cursor will single step in both directions and move smoothly when held to either the right or left step. Return cursor to left edge of screen, and Display to X1.	

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

Set up Front Panel controls as follows:

Record Mode - Delay Auto
Clock Source - Ext ∫

Set up one pulse generator for a 1 µsec wide pulse, 3 µsec repetition rate. Set the second pulse generator for a 50 MHz square wave out 0 to +3 V; use frequency counter to verify rate. Connect the output of the first pulse generator to the channel 1 input. Connect the output of the second pulse generator (50 MHz) to the EXT CLK input. 851-D should continuously arm, trigger, and record data. Display should be as shown in Figure 8.10. Increase the square wave rate to 60 MHz. No "spikes" or break up of data should occur. Repeat above procedure for all channels.

Waveform not as in Figure 8.10

Observe test point 17 for inputted CLK. Verify test points 42-49 for square wave outputs while synchronizing scope on (+) edges within gated waveform on each test point.

NOTE: Unit is recording and displaying over and over. The signals that are gated show this effect.

Change Front Panel controls as follows:

Clock Source - Int

No change in operation should be observed.

Change of waveform on display (break up).

Observe test point 17 for 0.02 µsec ECL clock.

8.37 Input Performance (CH 1-8)

Set Front Panel controls as follows:

Record Mode - Delay Man
Int Clock - 0.02 µsec
Clock Source - Int
Display - X1
Input Mode - Latch

CAUTION: CORRECT RESULTS WILL ONLY OCCUR IF THE TEST EQUIPMENT SPECIFIED AT THE BEGINNING OF THIS SECTION IS USED AND THE SETUP OF THIS TEST EQUIPMENT IS CAREFULLY FOLLOWED.

8.37 Input Performance (CH 1-8)

NOTE: All of the tests listed below are conducted with a 50 Ω termination at the input of the 851-D.

Set up the pulse generators as follows:

0 V to +2 V (0 V REF. Level)
5 nsec pulse width (measured at +1.5 V)
200 nsec pulse repetition rate

Input this pulse to channel 1. Press the MAN ARM button. A continuous group of pulses should be stored in the 851-D and displayed as shown in Figure 8.11. There should be no gaps or breakup in the pulse train. Place Combinational Trigger of channel selected to "1", then after checked return to "X". Repeat this step for all eight channels.

Waveform not as in Figure 8.11.

Verify ECL Logic Lo at test point 58. Monitor test points 70 and 71 for waveform (some jitter) with same repetition rate as input signal. Observe test point 72 for proper threshold setting "TTL". Repeat observation of all channels that don't meet specification. Observe test point 60 for ECL Lo.

Set up the pulse generator as follows:

+3 V to +1 V (+3 V REF. Level)
5 nsec pulse width (measured at +1.5 V)
200 nsec pulse repetition rate

Input this pulse to channel 1. Press the MAN ARM button. A continuous group of pulses should be stored and displayed as in Figure 8.12. Repeat this step for all eight channels and verify the proper operation.

Waveform not as in Figure 8.12.

Verify signals at test point 73 (same signal as input: High to low signal).

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
8.37 Input Performance (CH 1-8)	
Place 851-D in Sample Mode and set up the pulse generator as follows: 0 V to +2 V (0 V REF. Level) 25 nsec pulse width (measured at +1.5 V) 200 nsec pulse repetition rate	
Input this pulse to channel 1. Press MAN ARM button. A continuous row of pulses should be observed on the CRT. There should be no gaps or breakups in this pulse train. Continue this procedure for all eight channels.	Waveform has dropped bits. Check test point 58 for ECL Logic High Level. Verify test points 70 and 71 for ECL Logic Lo level. Observe test points 68 and 69 for a signal that has some jitter, but resembles input signal.
Set up pulse generator as follows: +3 V to +1 V (+3 V REF. Level) 25 nsec pulse width (measured at +1.5 V) 200 nsec pulse repetition rate	
Input this pulse to channel 1. Press the MAN ARM button. A continuous row of pulses should be displayed on the CRT, like the previous step, except the pulses will be high level to low (pulse width). Repeat this procedure for all eight channels.	Waveform has dropped bits. Observe test points 68 and 69 for input signal with jitter.
Place 851-D in Latch Mode and the Threshold (CH 1-4 & CH 5-8) to ECL X1. Set up pulse generator as follows: -1.8 V to -0.8 V (-1.8 V REF. Level) 5 nsec pulse width (measured at 0.3 V) 200 nsec pulse repetition rate	
Input this pulse in channel 1. Press MAN ARM button. A continuous row of pulses should be viewed on the CRT. Continue this check until all eight channels have been verified.	Waveform not correct. Check test point 72 for proper threshold "ECL". Check test point 74 for -12 mV level without signal inputted.

DIAGNOSTIC PROCEDURE	TROUBLESHOOTING PROCEDURE
Set up pulse generator as follows: -0.8 V to -1.8 V (-0.8 V REF. Level) 5 nsec pulse width (measured at -1.3 V) 200 nsec pulse repetition rate	
Input this pulse to channel 1. Press MAN ARM button. A continuous row of pulses should be stored in 851-D and displayed on the CRT. The pulses should look like the inverse of the previous step. Verify all eight channels as described for channel 1.	Waveform not correct. Observe test points 73 and 75 for input signal. Test points 73 and 75 will be inverse signals.
Place 851-D in Sample Mode, and set up pulse generator as follows: -1.8 V to -0.8 V (-1.8 V REF. Level) 25 nsec pulse width (measured at -1.3 V) 200 nsec pulse repetition rate	
Input this pulse to channel 1. Press MAN ARM button. A continuous row of pulses should be displayed. Repeat this procedure for all eight channels, verifying results.	Waveform not correct. Check test point 58 for ECL High Logic Level. Check same test points as in "TTL" test.
Set up pulse generator as follows: -0.8 V to -1.8 V (-0.8 V REF. Level) 25 nsec pulse width (measured at -1.3 V) 200 nsec pulse repetition rate	
Input this pulse to channel 1. Press MAN ARM button. A continuous row of pulses should be displayed like the previous step except inverted. Continue this procedure for all eight channels and verify results.	Waveform not correct. Check all test points as in "TTL" tests and recheck pulse generator for proper settings.
THIS COMPLETES THE DIAGNOSTIC PROCEDURE FOR THE 851-D.	

8.4 Disassembly Procedure

The following are disassembly procedures for the Model 851-D Front Panel and Power Supply sub-assemblies.

8.41 Front Panel

Disconnect power cord.
Remove top and bottom covers (four screws in each).
Remove four #6 hex nuts from inside the Front Panel (one in each corner).

Use a long 1/4 in. Spintite for removing the hex nuts.

Unplug the ribbon cables from the sockets. Unplug the power switch connector from the mating connector with the aid of a flat blade screwdriver. Stand unit up vertically and let it rest on the rear panel. Gently pull Front Panel upward while using the other hand to push it away from the connector (Control Board). For reassembly, reverse the above procedure.

8.42 Front Panel Sub-assembly

If it is necessary to disassemble the Front Panel to replace a component, proceed as follows:

Digitswitch Board

Place levers to midposition.
Remove four #6 screws.

NOTE: There is a cable that connects the digitswitch board to the main Front Panel that must remain on unless defective.

Front Panel Main Board

Remove four #4 screws from lower right.
Remove two #6 screws from left side.
Using a plier, grip side of the four remaining screws. Standoff and gently rotate to remove. Using 1/16 Allen head wrench, remove two Allen head screws from the three switch knobs on Front Panel.

8.43 Power Supply

Disconnect the power cord.
Remove power cable connector from main board.

Remove four #4 screws from angle bracket connecting Power Supply to case. On the rear panel remove the four #4 screws from edges of power supply rear panel (there appears to be two sections to rear panel).

NOTE: Be very careful on the position of the next screws to be removed because the fan does not have to be removed from the Power Supply sub-assembly. There are four #6 screws that support the rear fan grill that do not need to be removed.

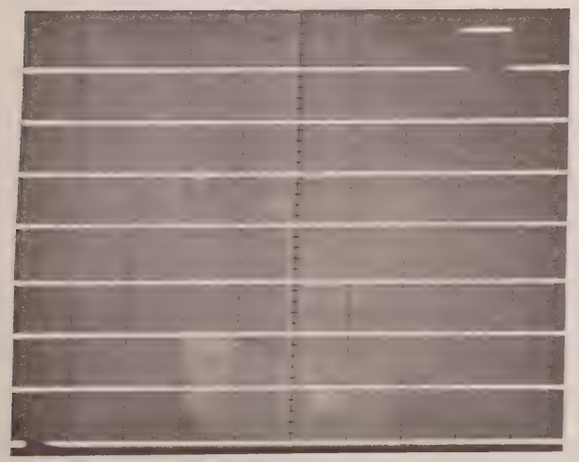
Slide power supply assembly from case, being careful not to break any wires.

8.44 Power Supply Sub-assembly

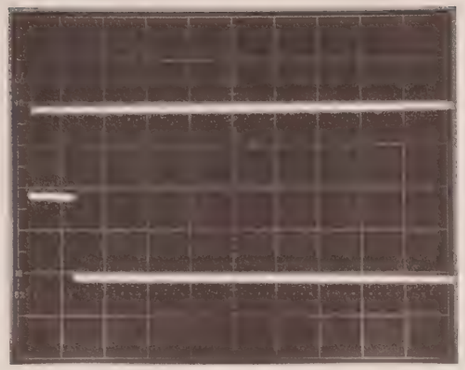
If it is necessary to disassemble the power supply regulator card, proceed as follows. Remove the four #4 mounting screws from corners of PC Board. Remove the four #6 screws on the regulator board that hold pass transistors to the board on the rear side. Lift out the two transistors from their respective sockets. The board is now ready for service or the main components of the Power Supply. For reassembly, reverse the above procedure.

8.1

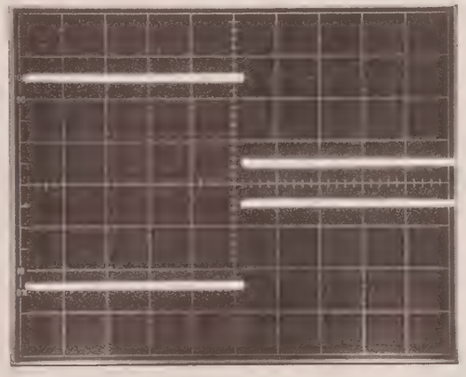
8.2



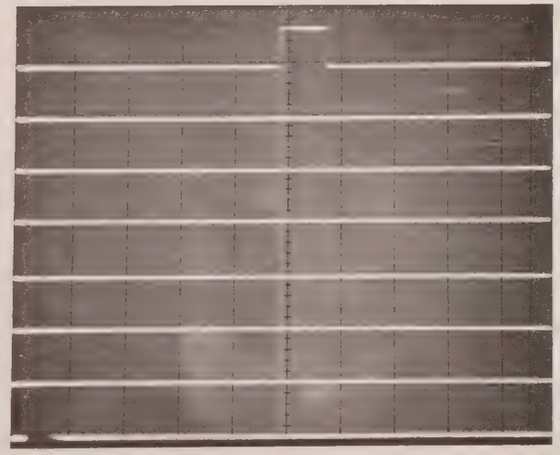
8.3



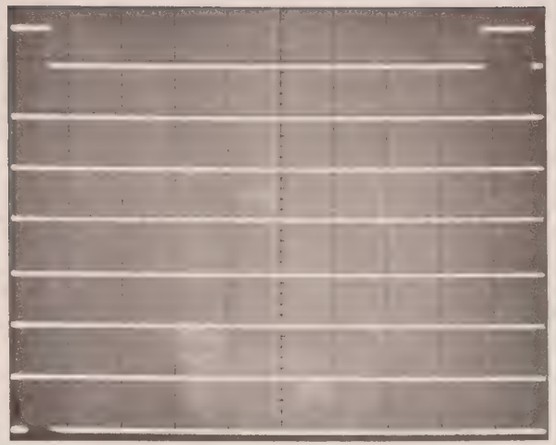
8.4



8.5

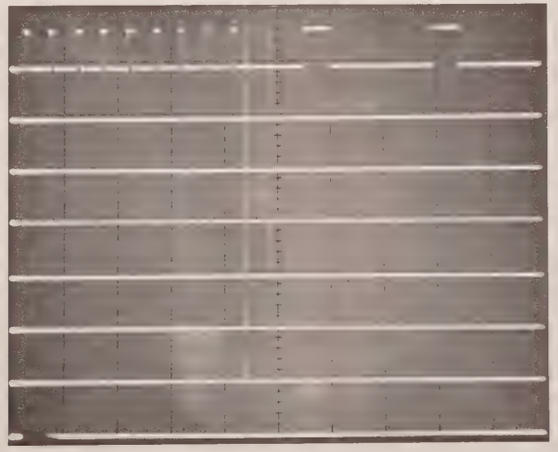


8.6



8.7

8.8



8.9

8.10

8.11

8.12

SECTION IX

SCHEMATICS AND ASSEMBLY DRAWINGS

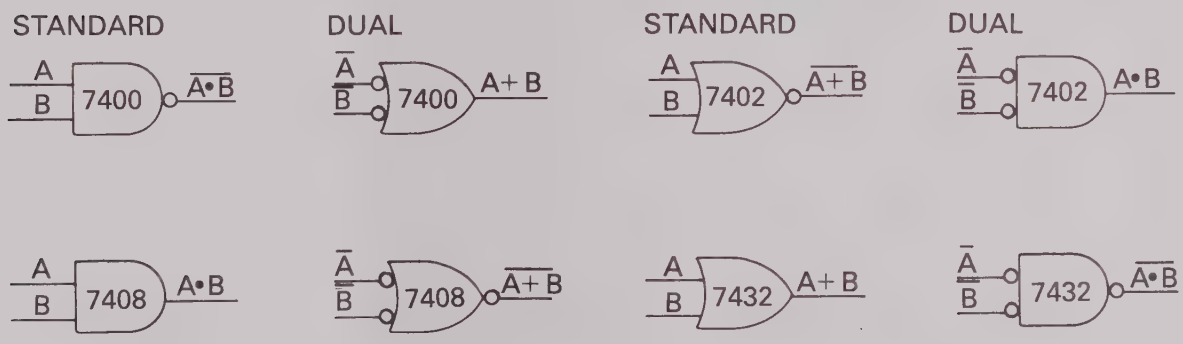
9.1 Introduction

This section contains the schematics and assembly drawings for the Model 851-D. Test points and waveform photographs are included, along with internal photographs of the unit.

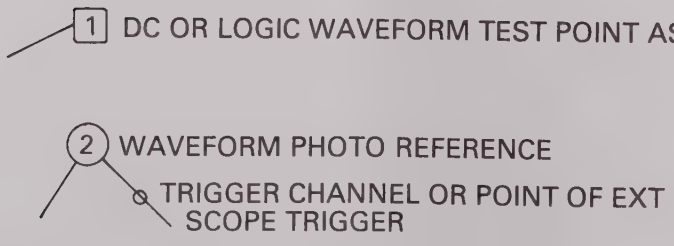
9.2 Logic Symbols and Reference Designators

LOGIC SYMBOLS

The Logic Symbols used in this manual depict the logic function performed and may be different than those published in the manufacturers' data book.



REFERENCE DESIGNATORS



9.3 List of Drawings

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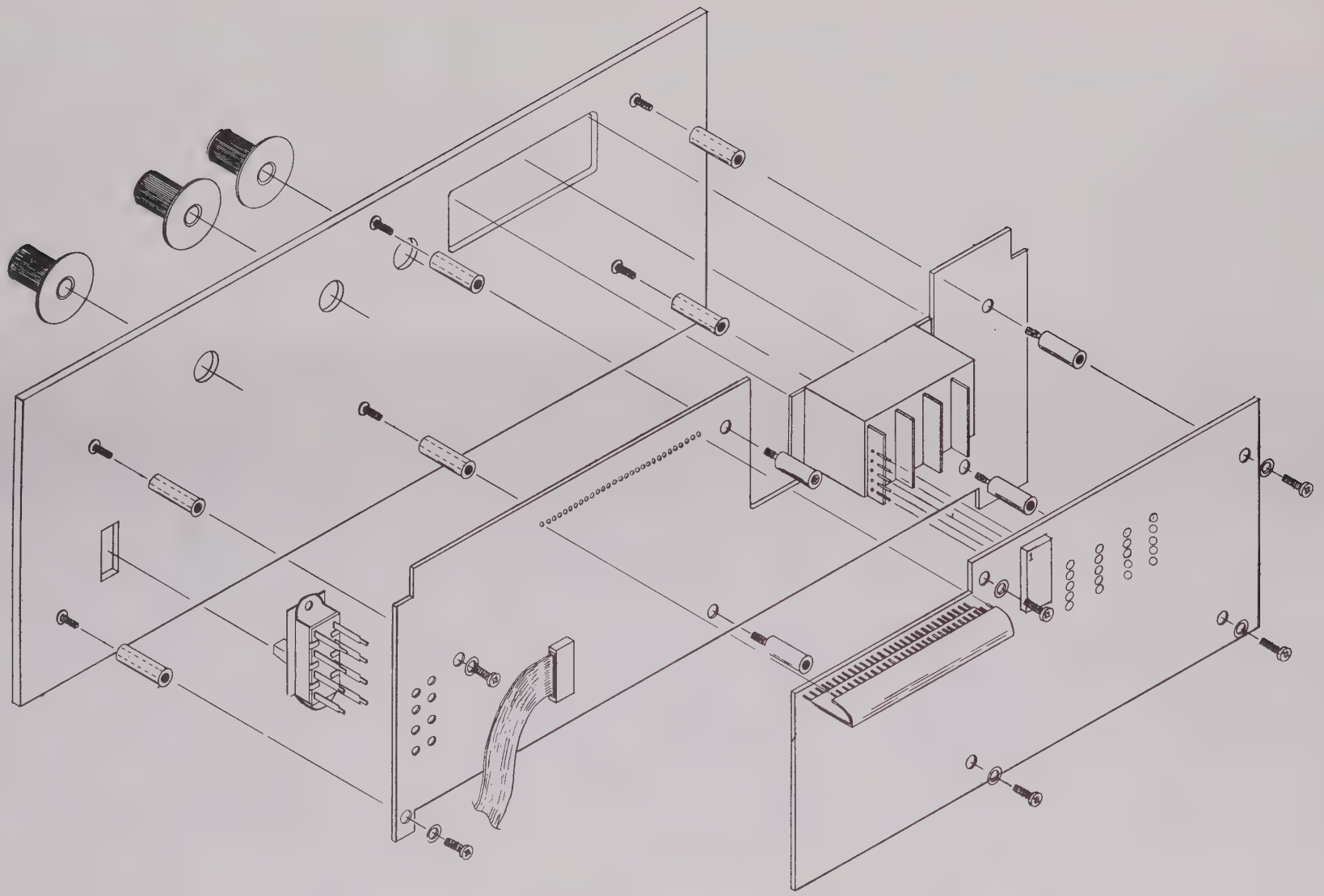


Figure 9.1 Front Panel Assembly Drawing

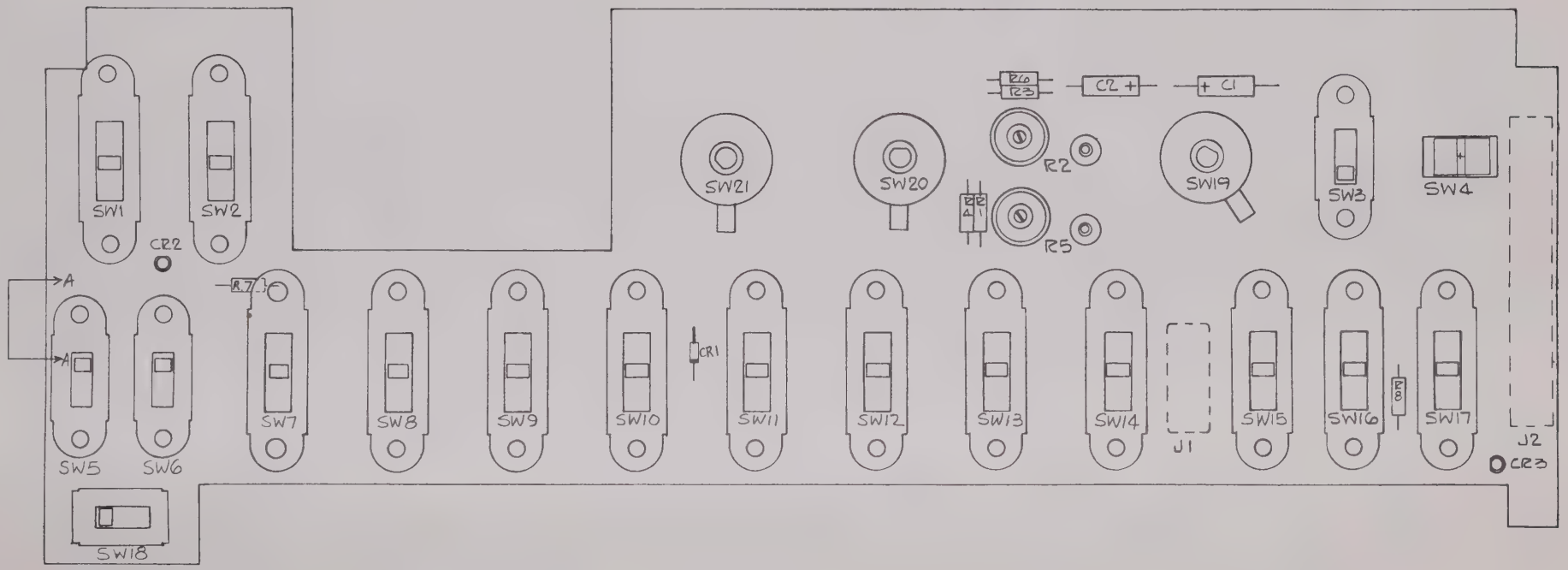


Figure 9.2 Front Panel PWB Assembly Drawing

REV D REDRAWN TO INCLUDE 0852-0086 ECN 503

X1000 MOST SIGN. DIGIT | X100 | X10 | X1 LEAST SIGN. DIGIT | DIGIT SWITCH BD 0852-0086

J1 TO J3(MB)

GND

INT. CLK. PERIOD

20 → J2-5
10 → J2-H
5 → J2-8
2 → J2-9
1 → J2-L
.5 → J2-K
.2 → J2-J
.1 → J2-7
.05 → J2-F
.02 → J2-E

EXPAND POSITION

CLOCK
m SEC

LEFT → J2-3
RIGHT → J2-D

m SEC → J2-6

m SEC

TRIG SOURCE
INT T
INT F
EXT

RECORD MODE
PRE-TRG.
DELAY MAN
DELAY AUTO

DELAY AUTO → J2-M
PRE-TRIG → J2-10
TRG EXT. → J2-N
TRG INT(T) → J2-11

J1 TO J4(M.B.)

MAN. ARM
N.C.
N.O.

MAN. TRIG
N.C.
N.O.

INPUT MODE
LATCH
SAMPLE

1 | X | 0

CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8

COMBINATIONAL TRIGGER

1N4152 CR1

INT
EXT ⌋
EXT ⌈
CLOCK SOURCE

X5
X10
X20
HORIZONTAL DISPLAY

X1
MIX
EXP

CK INT → J2-15
CK EXT ⌈ → J2-T
X5 → J2-S
X20 → J2-16
X1 → J2-14
EXPAND → J2-U

GND → J2-R

CR3 POWER ON LIGHT

MAN TRIG → J2-V
LATCH → J2-18
MAN ARM → J2-2
MAN ARM → J2-17

FRONT PANEL

DIGITSWITCH P.W.B.
0852-0086

NOTE READINGS TAKEN WITH THRESHOLD SET TO "TTL"

X10 C 26
X10 B 24
X10 A 21
X10 MST 22
X10 TTL 23
X10 ECL 25
VAR 30
MST 27
TTL 28
ECL 29
5-8 COMMON 9
VAR 13
1-4 ADJ 7
5-8 ADJ 10

1-4 COMMON 8
ECL 11
TTL 12
MST 16
X10 ECL 17
X10 TTL 18
X10 MST 19
X10 A 20
X10 B 15
X10 C 14

R9 10K
R8 10K
R7 10K
R6 10K
R5 10K
R4 10K
R3 10K
R2 10K
R1 2K CW 1 CCW
R11 1.65K
R10 1.65K +5V
R12 20K
C3 1μfd/35V

U1 1458
+.52
R13 2K
R14 20K
R15 20K
+5V
-5.2
-.51

C1 10μfd/20V
+5V
J2 5-A

U2 1458
+1.41
4-C
3-12
2-4
1-P

-5.2V
6-1
C2 10μfd/20V

180Ω, 5% R7
CR2 TRIG READY LIGHT
ARMED LIGHT → J2-13

C1 10μfd 20V
C2 10μfd 20V
R8 180Ω
-5.2V → J2-1
+5V → J2-A

R1 499Ω, 1%
R2 1K
VARIABLE "1"
R3 499Ω, 1%
VARIABLE "0"
R4 499Ω 1%
R5 1K
R6 499Ω, 1%

Figure 9.3 Front Panel Schematic

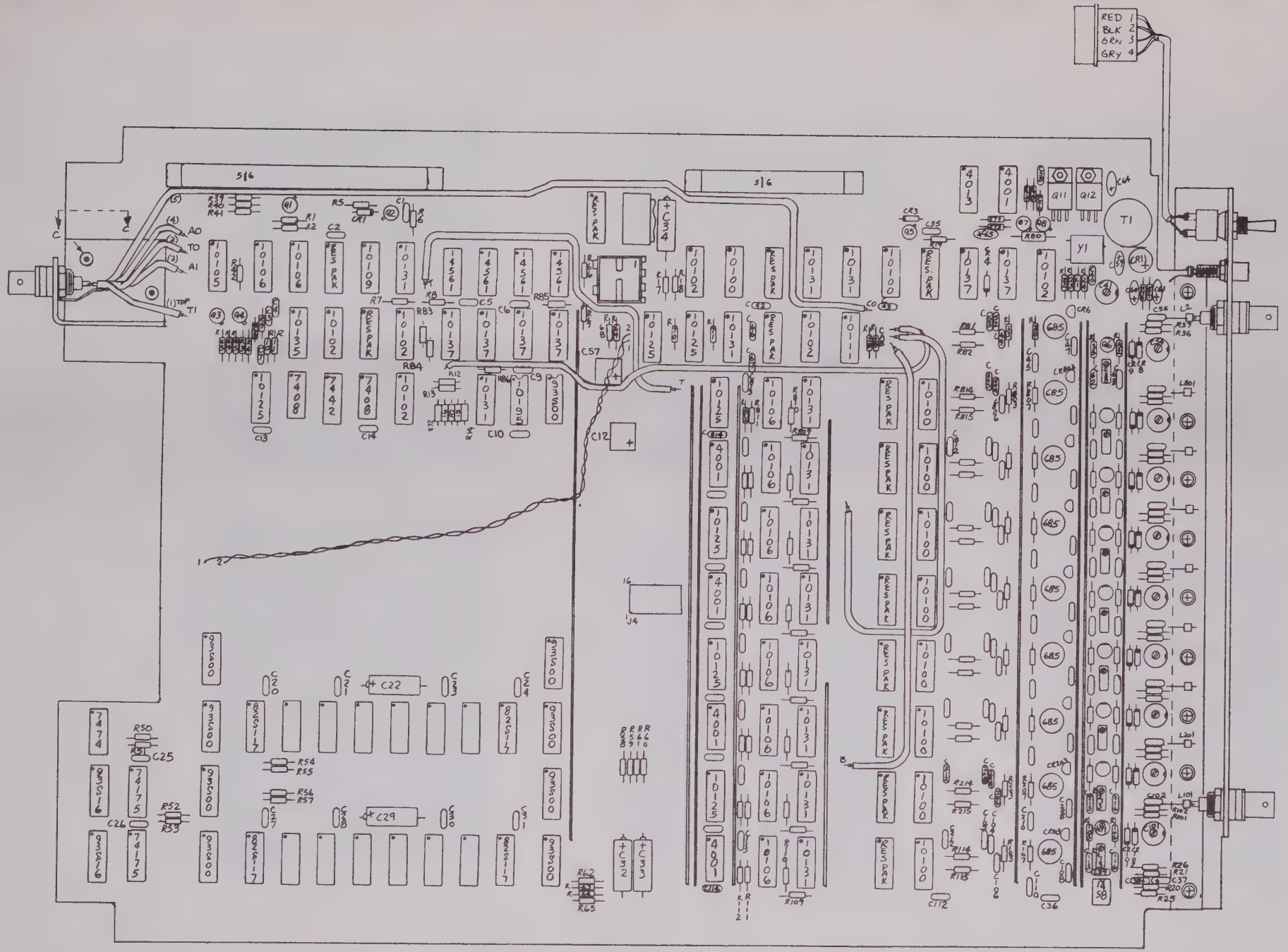
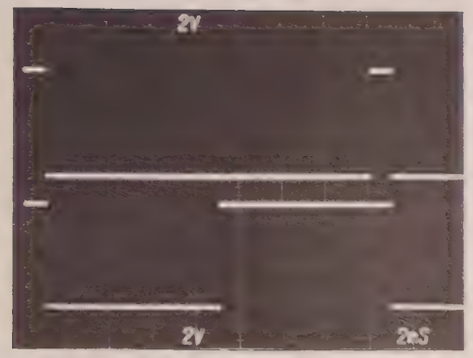
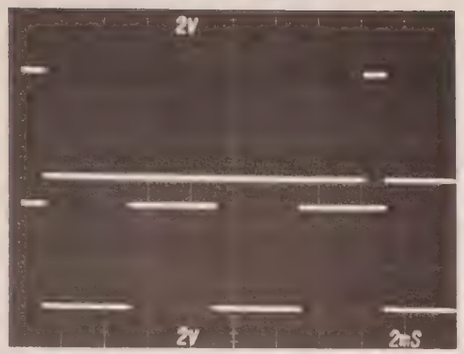


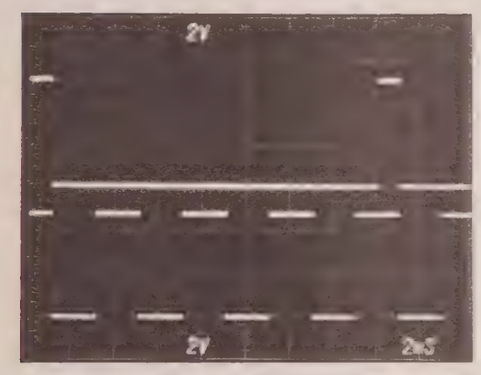
Figure 9.4 Main Board Assembly Drawing



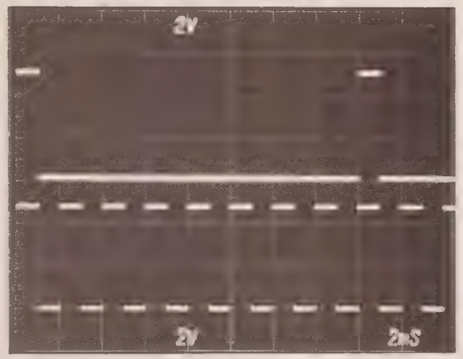
1. TEST POINT 1
SCOPE: CHANNEL A (+)



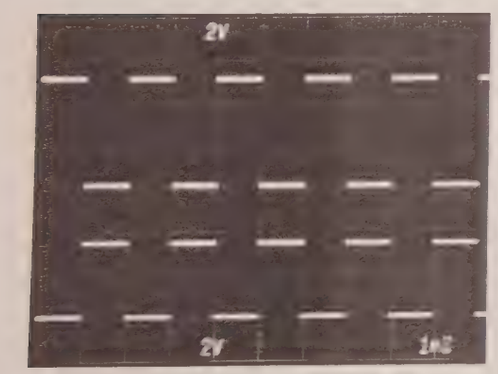
2. TEST POINT 2
SCOPE: CHANNEL A (+)



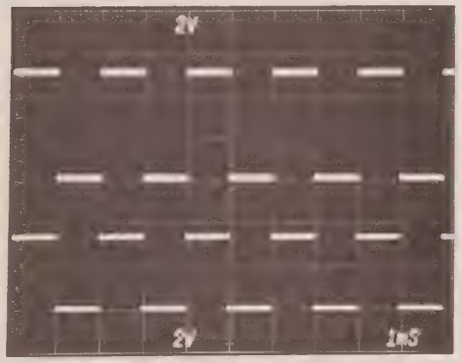
3. TEST POINT 3
SCOPE: CHANNEL A (+)



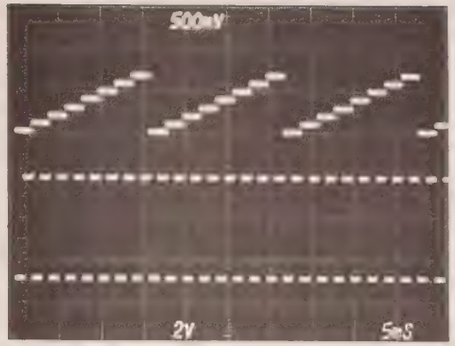
4. TEST POINT 4
SCOPE: CHANNEL A (+)



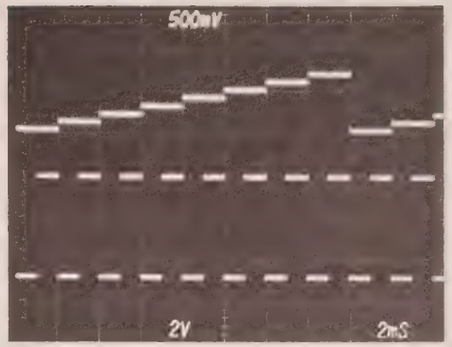
5. TEST POINT 7
SCOPE: CHANNEL A (+)



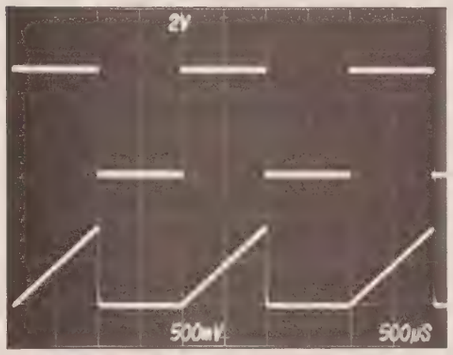
6. TEST POINT 6
SCOPE: CHANNEL A (+)



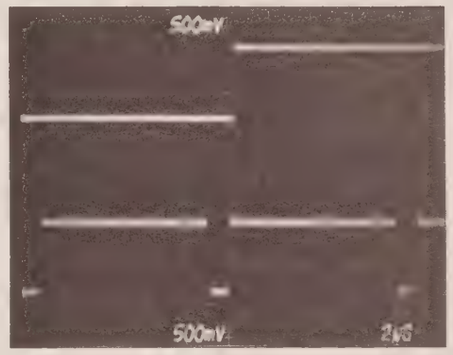
7. TEST POINT 8
SCOPE: CHANNEL A (−)



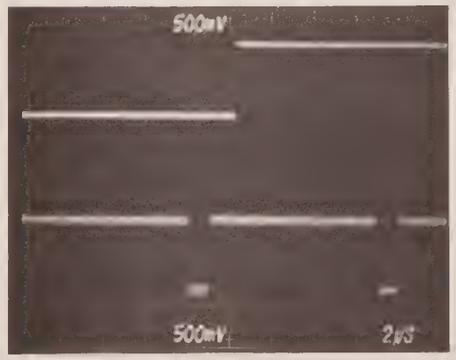
8. TEST POINT 8
SCOPE: CHANNEL A (−)



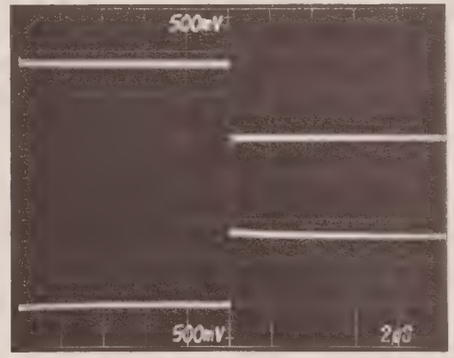
9. TEST POINT 9
SCOPE: CHANNEL A (+)



10. TEST POINT 10
SCOPE: CHANNEL A (−)

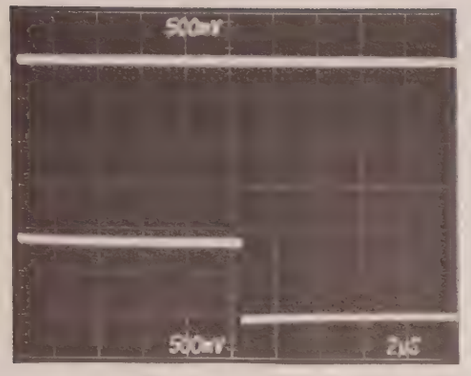


11. TEST POINT 10
SCOPE: CHANNEL A (−)

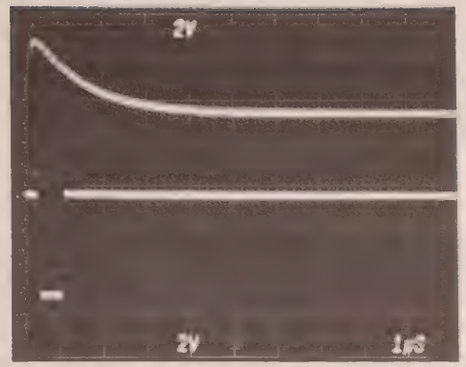


12. TEST POINT 30
SCOPE: CHANNEL A (+)

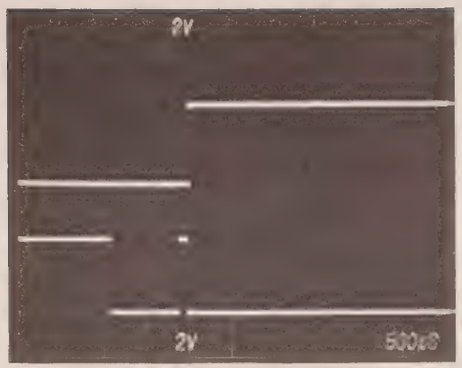
Figure 9.5 Waveform Photographs



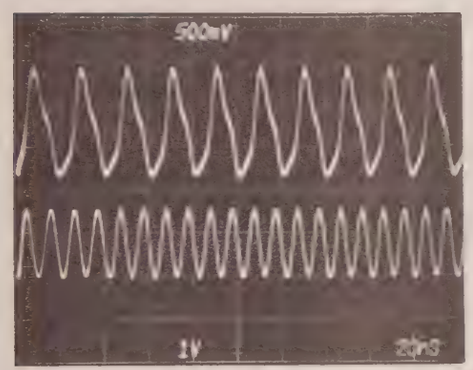
13. TEST POINT 29
SCOPE: CHANNEL A (−)



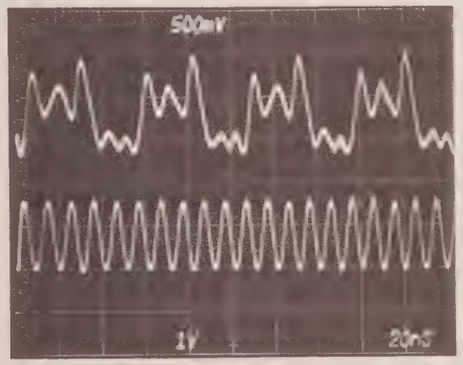
14. TEST POINT 33
SCOPE: CHANNEL A (+)



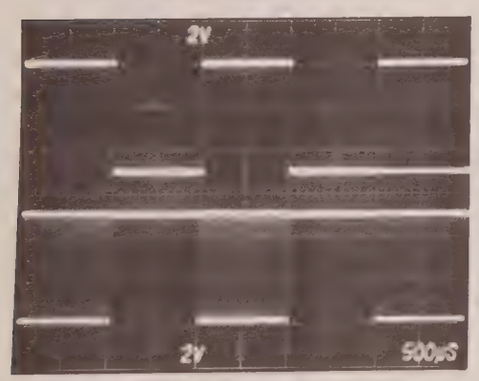
19. TEST POINT 37
SCOPE: CHANNEL A (−)



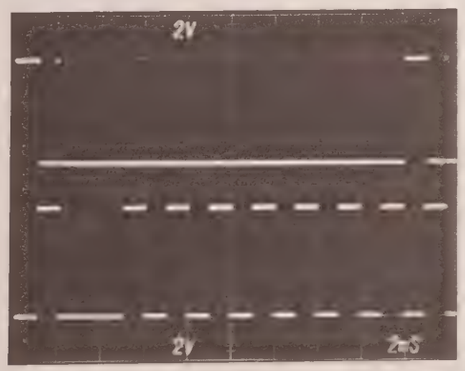
15. TEST POINT 15
SCOPE: CHANNEL A (+)



16. TEST POINT 16
SCOPE: CHANNEL A (+)



17. TEST POINT 34
SCOPE: CHANNEL A (+)



18. TEST POINT 39
SCOPE: CHANNEL A (+)

Figure 9.5 Cont. Waveform Photographs

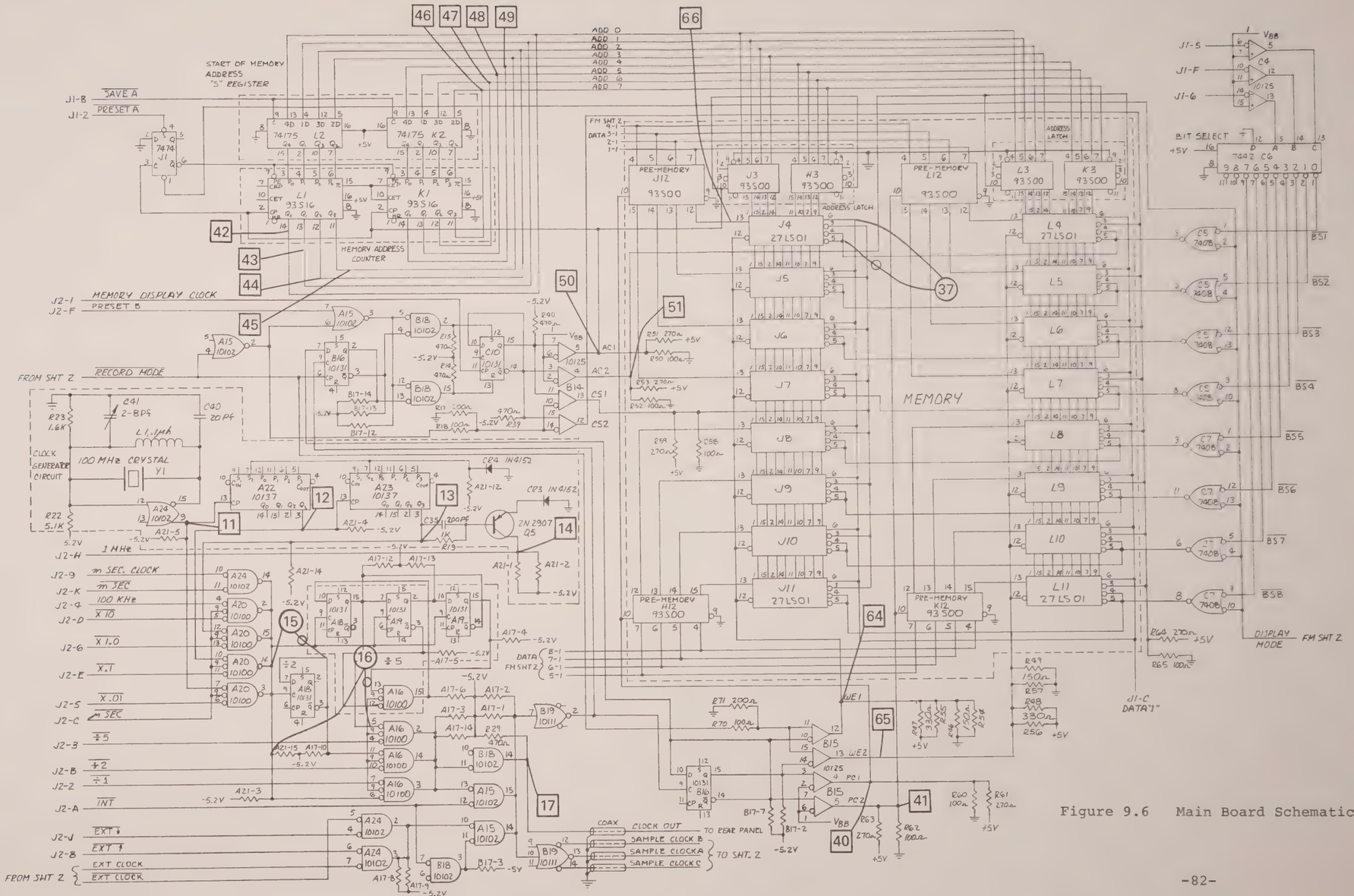
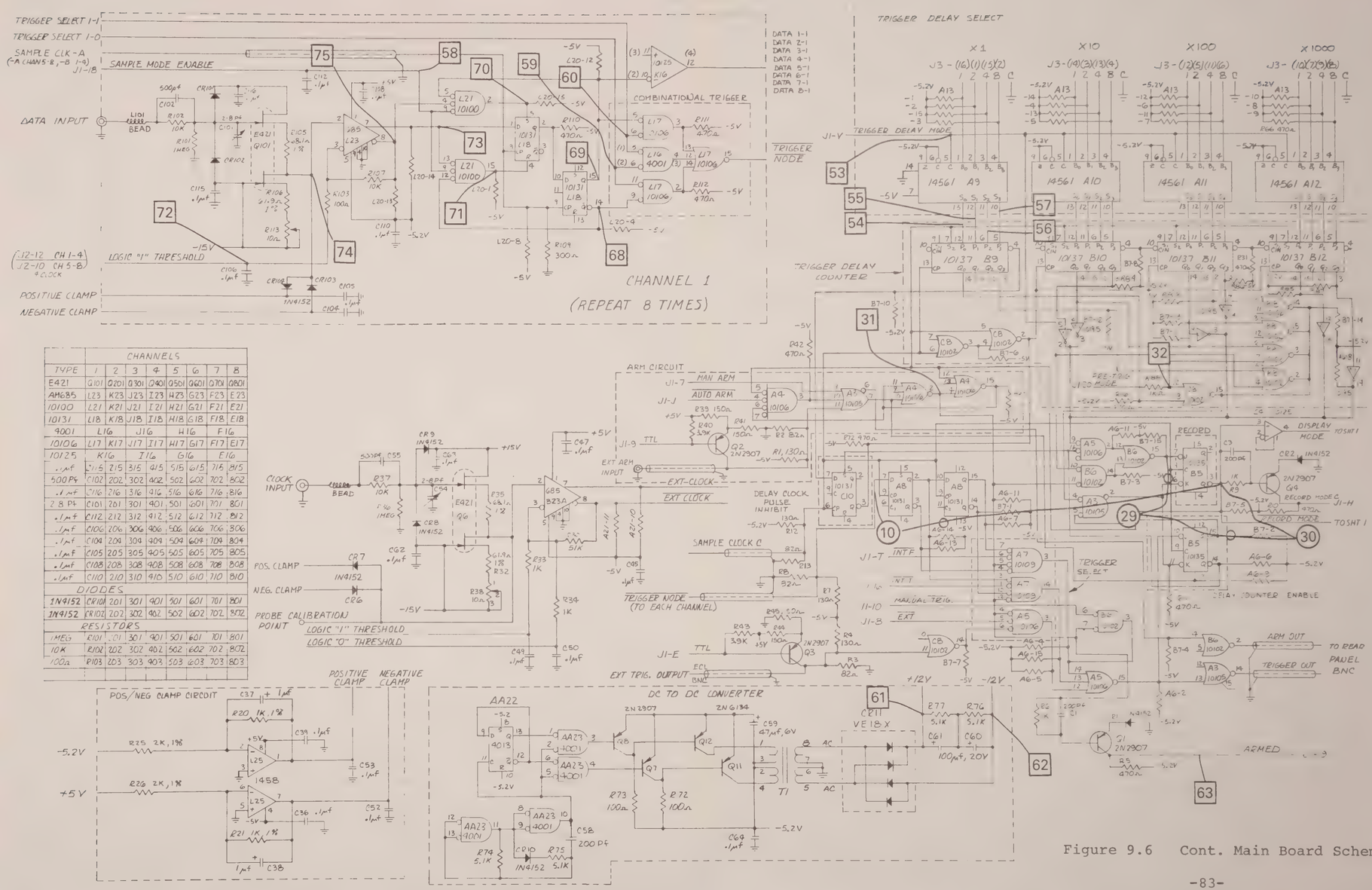


Figure 9.6 Main Board Schematic



	CHANNELS							
TYPE	1	2	3	4	5	6	7	8
E421	Q101	Q201	Q301	Q401	Q501	Q601	Q701	Q801
AM685	L23	K23	J23	I23	H23	G23	F23	E23
10100	L21	K21	J21	I21	H21	G21	F21	E21
10131	L18	K18	J18	I18	H18	G18	F18	E18
9001	L16		J16		H16		F16	
10106	L17	K17	J17	I17	H17	G17	F17	E17
10125	K16		I16		G16		E16	
.1 mf	115	215	315	415	515	615	715	815
500 PF	C102	202	302	402	502	602	702	802
.1 mf	C116	216	316	416	516	616	716	816
2-8 PF	C101	201	301	401	501	601	701	801
.1 mf	C112	212	312	412	512	612	712	812
.1 mf	C106	206	306	406	506	606	706	806
.1 mf	C104	204	304	404	504	604	704	804
.1 mf	C105	205	305	405	505	605	705	805
.1 mf	C108	208	308	408	508	608	708	808
.1 mf	C110	210	310	410	510	610	710	810
DIODES								
1N4152	CR101	201	301	401	501	601	701	801
1N4152	CR102	202	302	402	502	602	702	802
RESISTORS								
1MEG	R101	201	301	401	501	601	701	801
10K	R102	202	302	402	502	602	702	802
100Ω	R103	203	303	403	503	603	703	803

Figure 9.6 Cont. Main Board Schematic

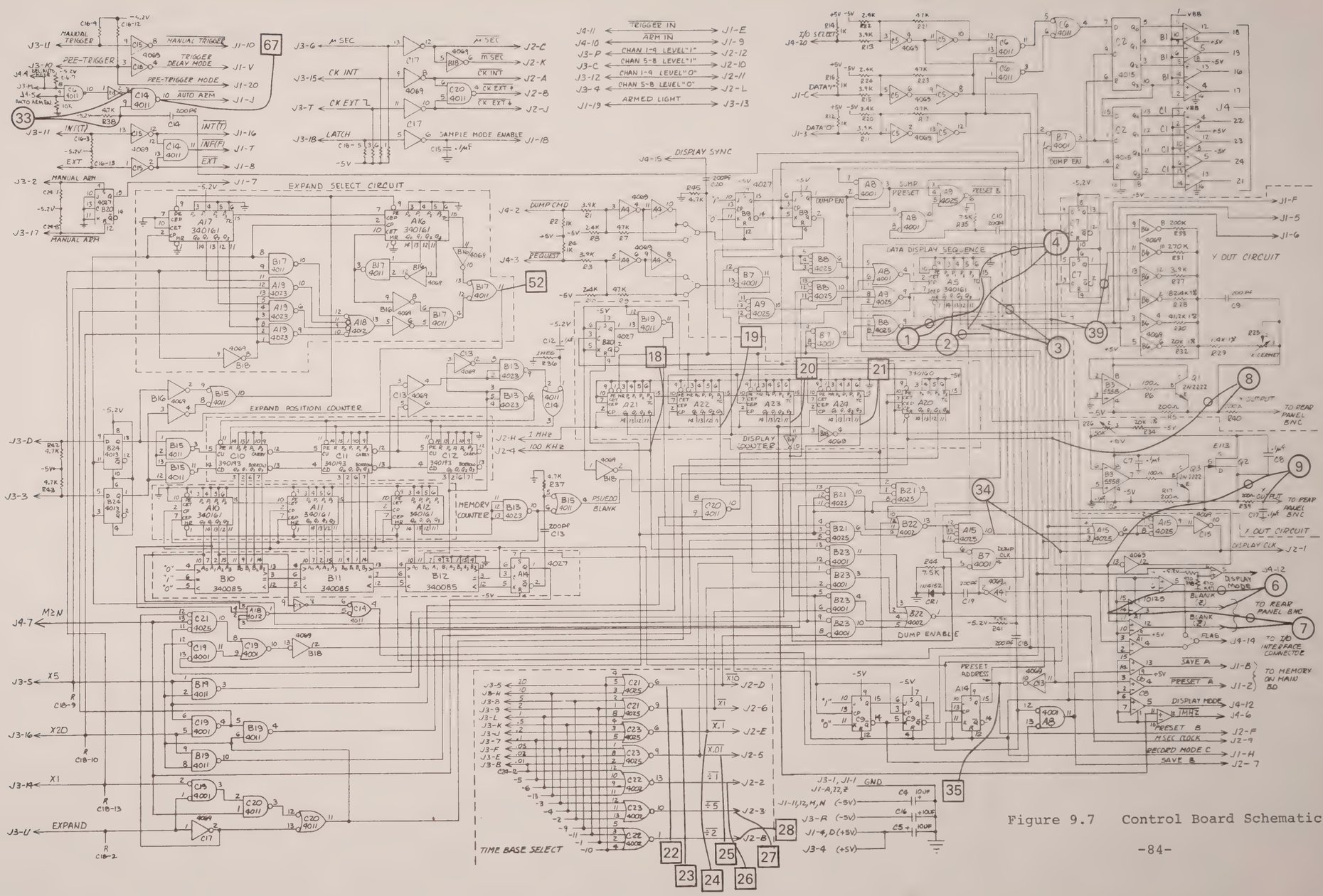
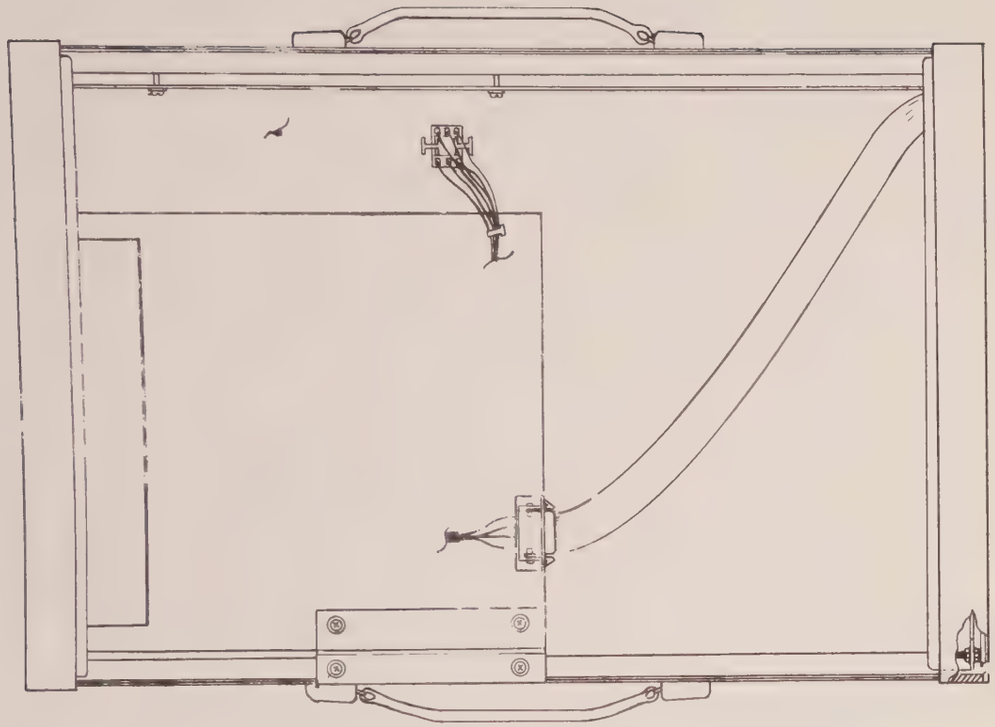
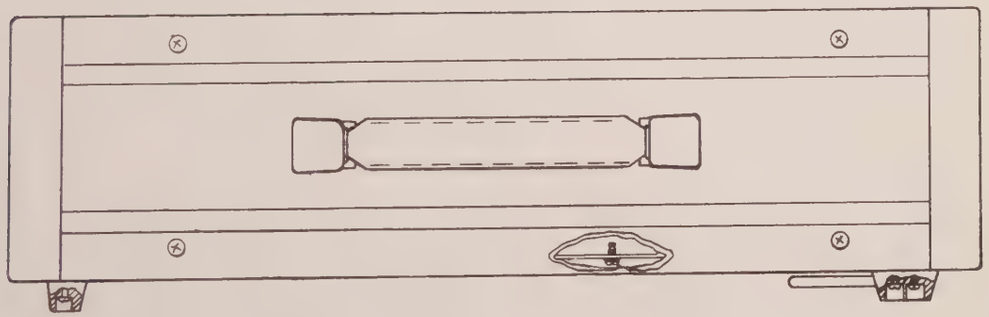


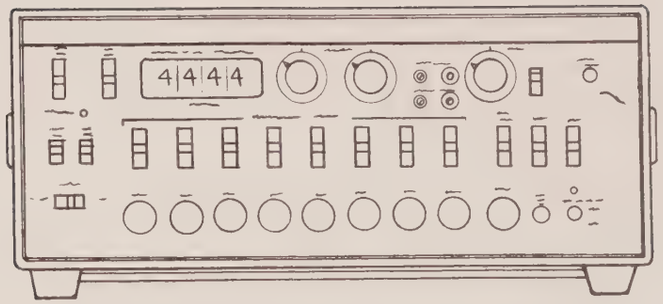
Figure 9.7 Control Board Schematic



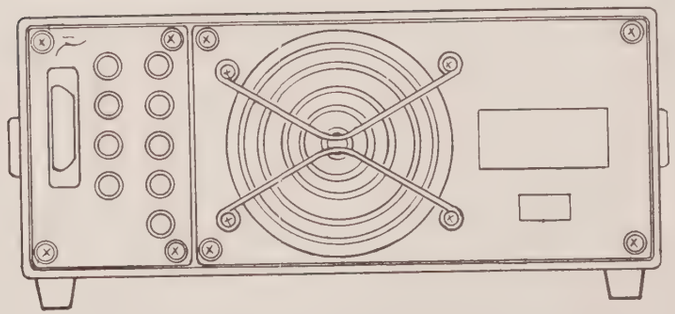
TOP VIEW



SIDE VIEW

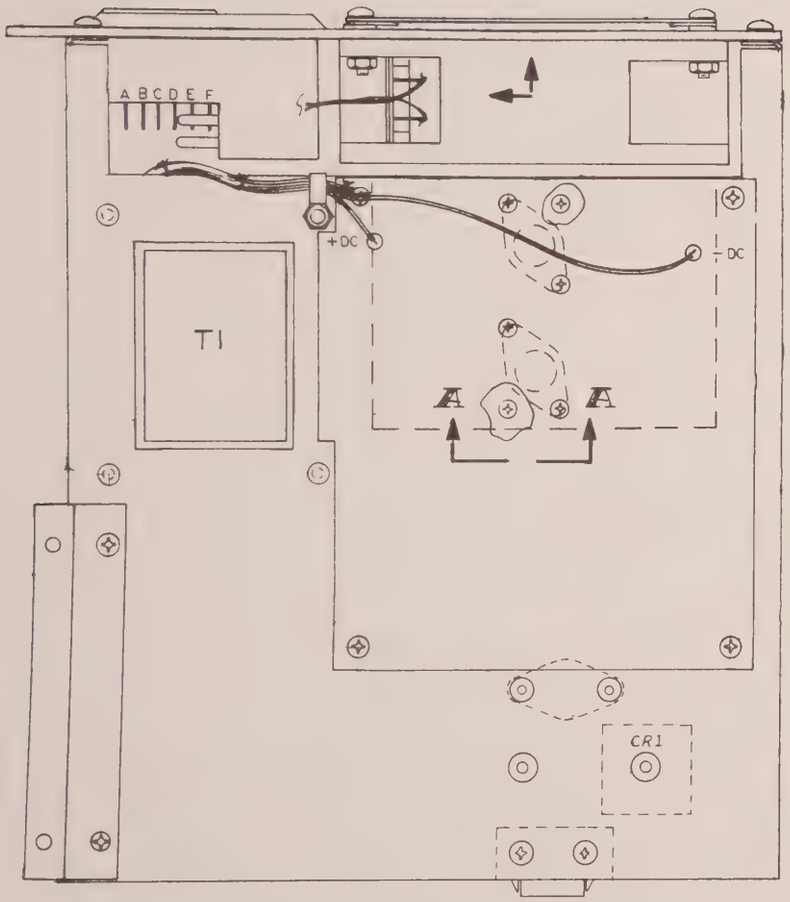


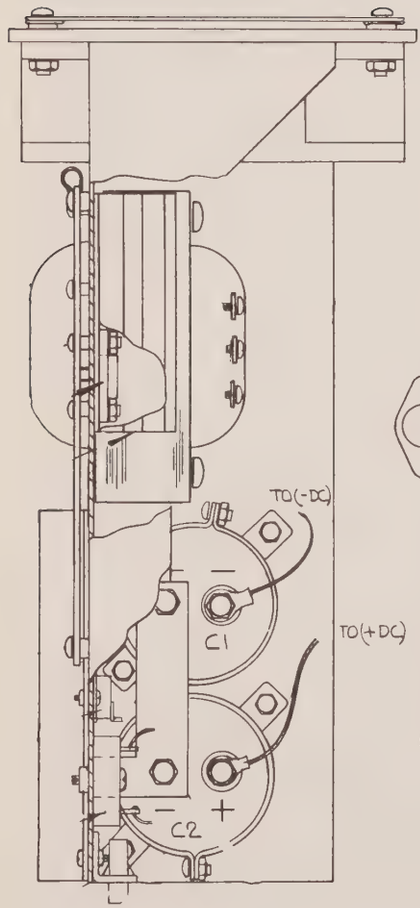
FRONT VIEW



BACK VIEW

Figure 9.8 Top Assembly Drawing





POWER WIRING DIAGRAM

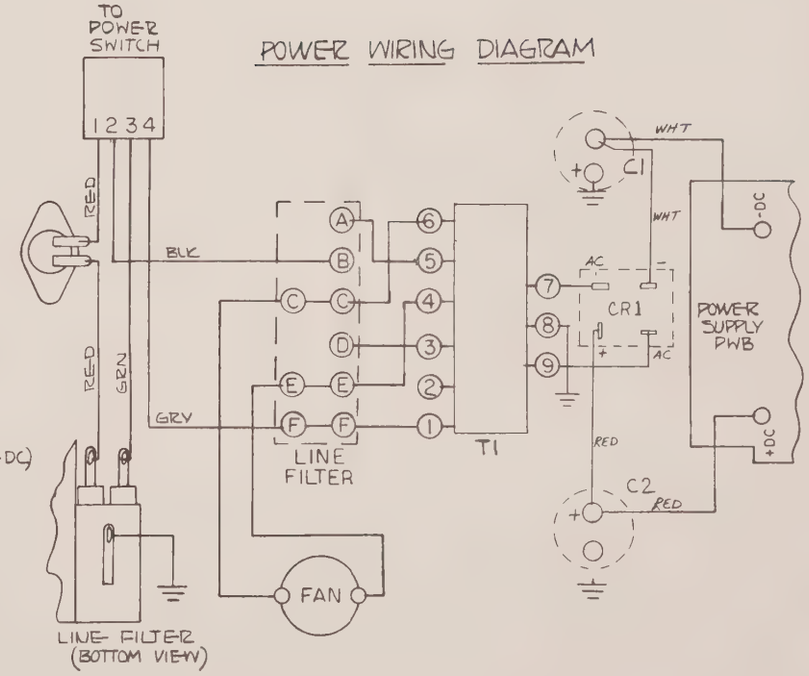


Figure 9.9 Power Supply Assembly Drawing

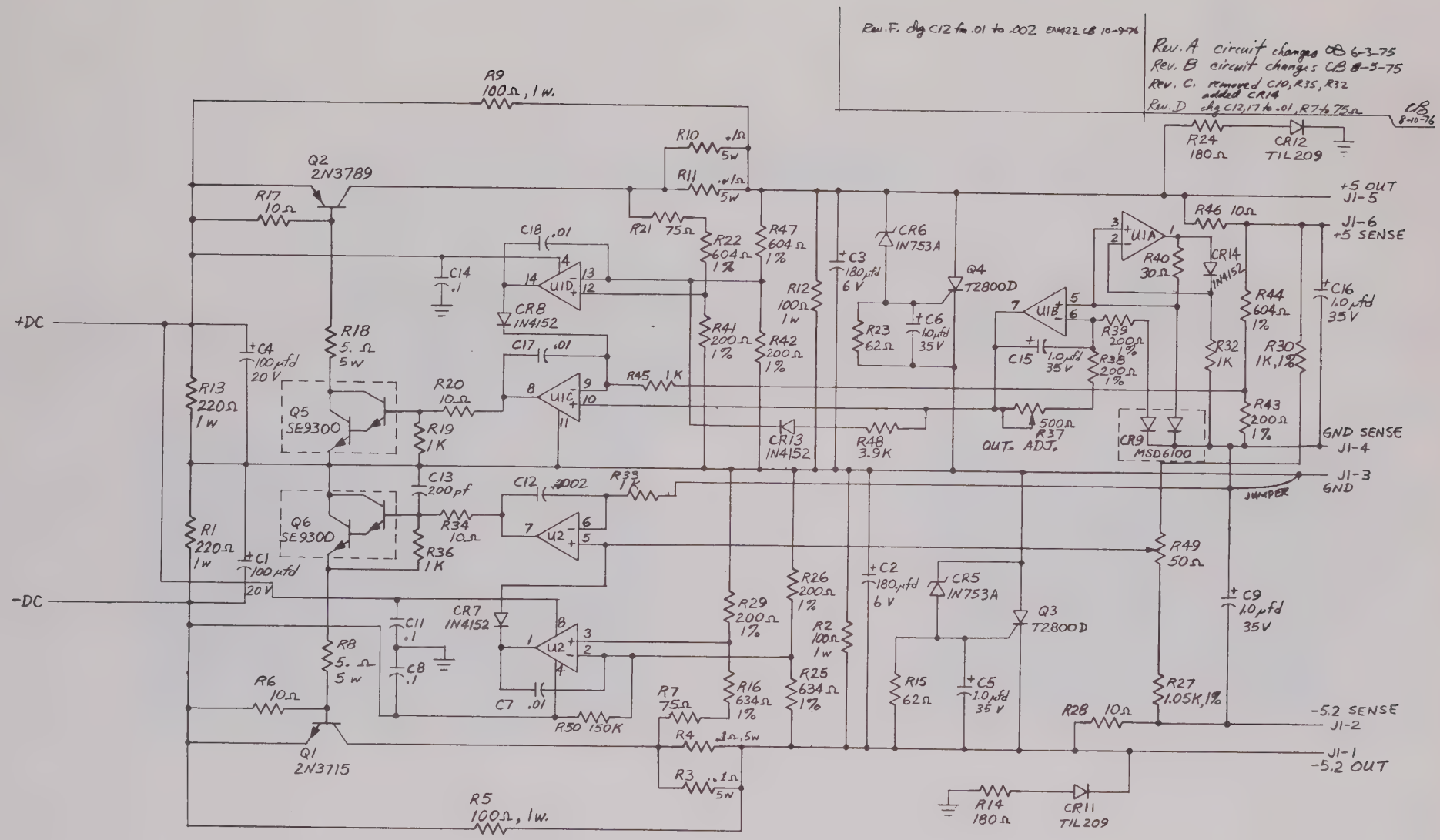
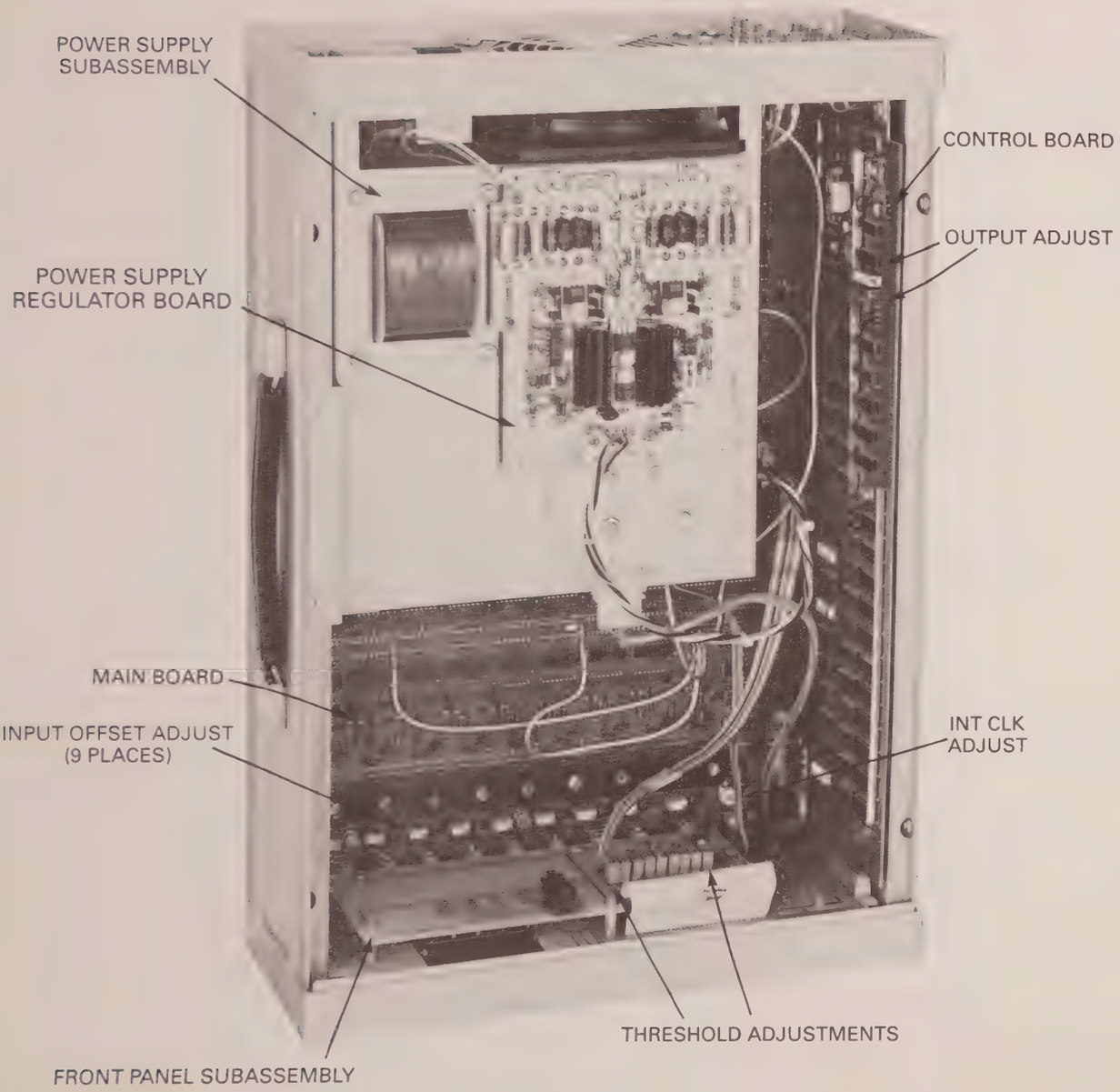
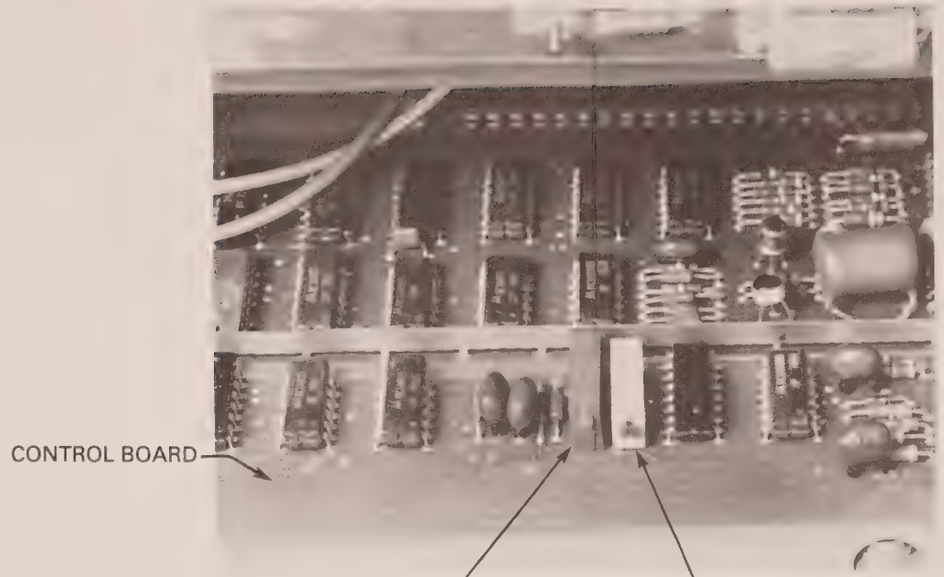


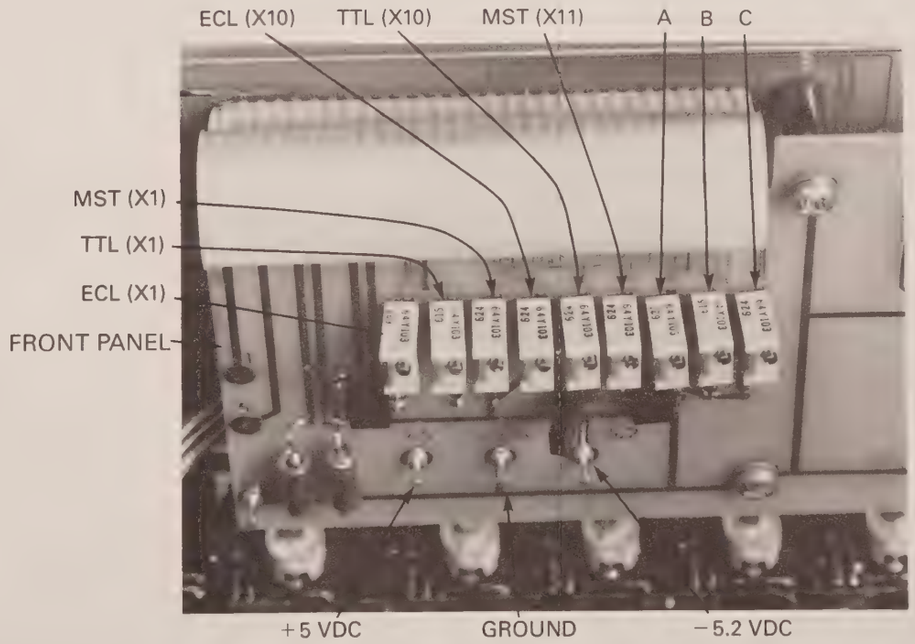
Figure 9.10 Power Supply Schematic



TOP INTERNAL VIEW
(TOP COVER REMOVED)

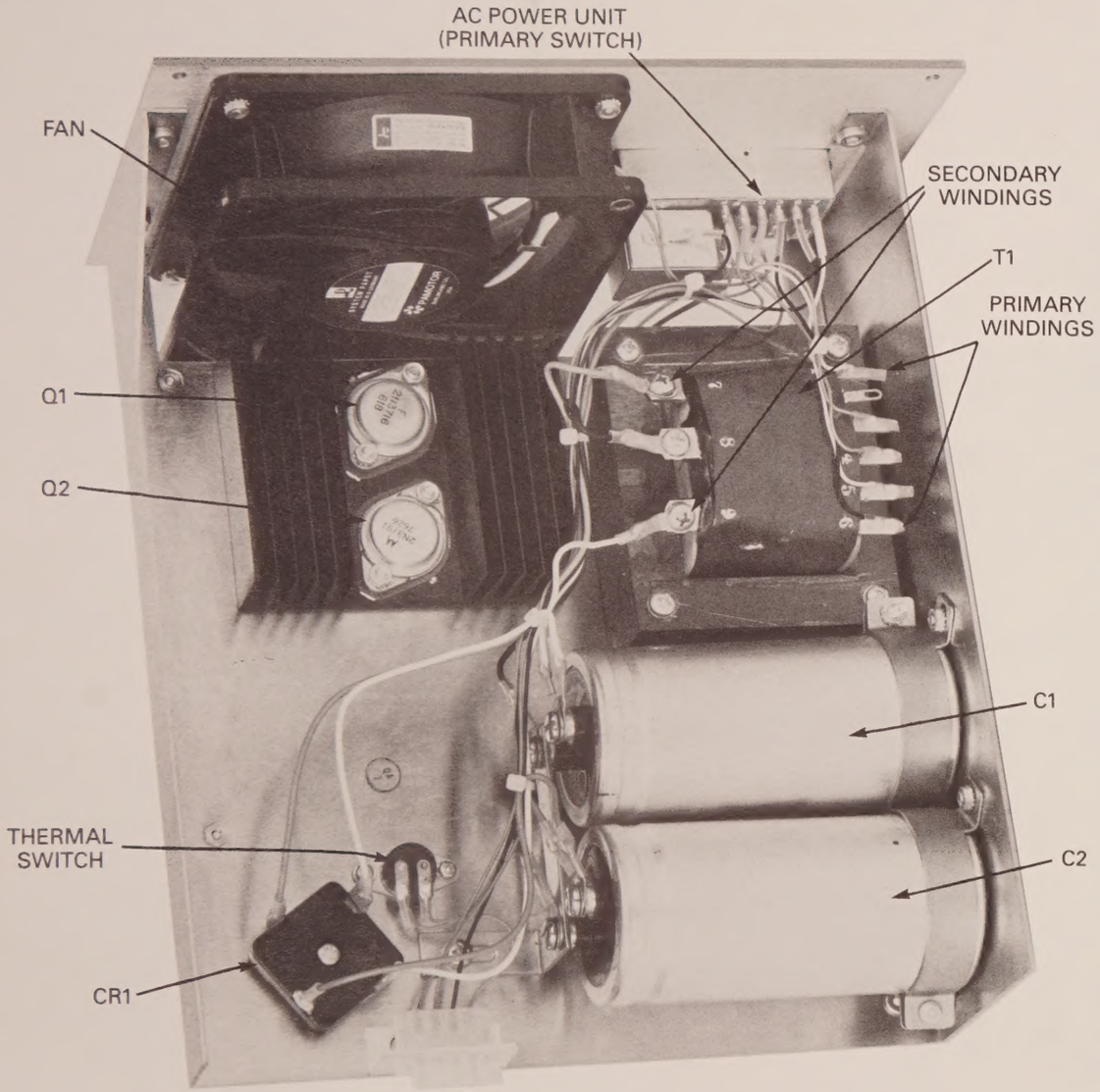


OUTPUT ADJUSTMENT

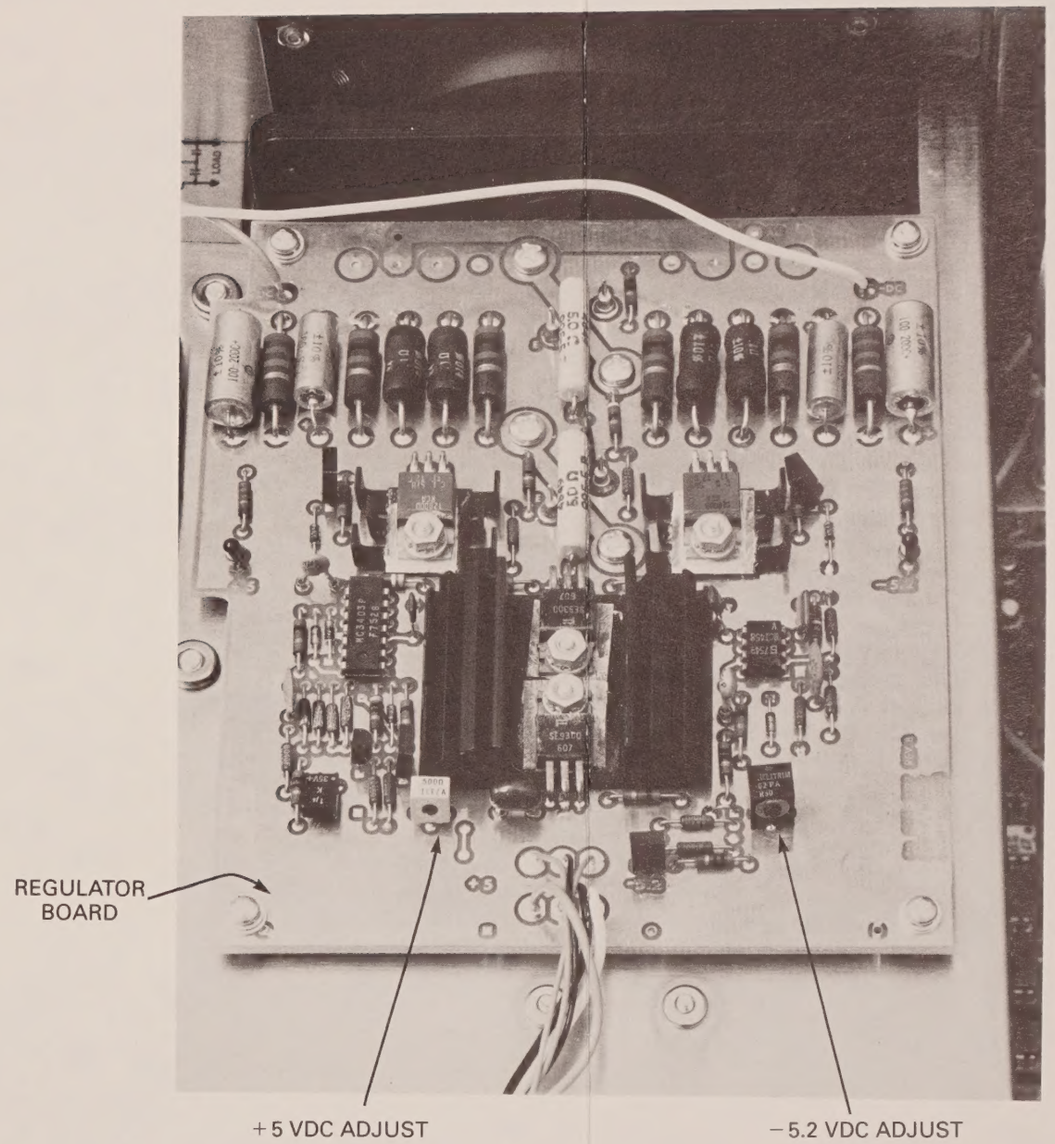


FRONT PANEL THRESHOLD ADJUSTMENTS

Figure 9.11 Internal Views



SIDE VIEW
(POWER SUPPLY REMOVED FROM UNIT)



POWER SUPPLY ADJUSTMENTS

Figure 9.12 Side View of Subassembly

MP MASTER
MA34613